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DESIGN AND FABRICATION OF GaAs MASK PROGRAMMABLE FUNCTIONS AND LOGIC ARRAY

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United States Air Force (AFSC)
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Bolling AFB, Washington DC 20332

C.G. Kirkpatrick
Program Manager

NOVEMBER 1985

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This program was to be implemented in three phases. During Phase I, a study was performed to determine the circuit elements to be developed, the gate technology to be used and speed/power analysis of basic circuit elements. In Phase IIA, the circuits identified as part of the Phase I study were designed, analyzed, processed and tested with the test results and packaged components to be delivered to ERADCOM.

Phase IIB was to be a repeat of Phase IIA, where new circuit designs would replace some of the original circuit elements. The Phase IIB effort was deleted from the program and the time/financial assets were applied to the task of detailed testing and analysis of the components developed under Phase IIA.

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TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

1.0 INTRODUCTION

This is the final report on the "Design and Fabrication of GaAs Mask Programmable Functions and Logic Array," program sponsored by ERADCOM for the development of basic circuit components applicable to high performance communication systems, particularly in the area of direct and indirect frequency synthesizers.

The program was to be implemented in three phases. During Phase I, a study was performed to determine the circuit elements to be developed, the gate technology to be used and speed/power analysis of basic circuit elements. In Phase IIA, the circuits identified as part of the Phase I study were designed, analyzed, processed and tested with the test results and packaged components to be delivered to ERADCOM.

Phase IIB was to be a repeat of Phase IIA, where new circuit designs would replace some of the original circuit elements. The Phase IIB effort was deleted from the program and the time/financial assets were applied to the task of detailed testing and analysis of the components developed under Phase IIA.

Three wafer lots (four wafers per lot) were processed; however, the majority of test data included in this report was obtained from wafers JE1-11 and JE1-14 of wafer lot number 1.

All program objectives were successfully met, except the thermal evaluation of devices to determine operational characteristics over the military temperature range of -55°C to +125°C.

2.0 CIRCUIT DEVELOPMENT

The circuit elements designed for the Phase IIA effort of this program were reported on in the "LSI/VLSI Ion Implanted Planar GaAs IC Processing" Semi-Annual Technical Report, for the period August 1, 1983 through January 31, 1984. The Rockwell document number is MRDC41129.6SA.

Data from the above report and other sources are included within this document for continuity without reference to previously submitted information.

Circuit designs were implemented using three basic approaches which included mask programmable functions, storage logic arrays and custom designs. Included with the circuit elements were numerous test structures for collection of parametric and processing data.

2.1 Mask Programmable Functions

To demonstrate the mask programming capabilities associated with the GaAs processing technology used in this program, a basic prescaler cell (Fig. 2.1-1) was developed and programmed to produce prescalers with the divide ratios, as listed in Table 2.1-1.

The programming technique involved via etches and second level metal interconnect to the first level metal.

2.2 Storage Logic Arrays (SLAs)

The second design approach used in the development of circuit elements encompassed the use of a storage logic array, which was composed of four basic structures: 1) 12 custom designed D flip-flops optimized for maximum performance (Fig. 2.2-1); 2) basic discrete devices for implementation of random logic (Fig. 2.2-2); 3) standard gate structures implemented with the transistor/diode elements (Fig. 2.2-3); 4) input receivers (Fig. 2.2-4); and 5) output driver circuits (Fig. 2.2-5).

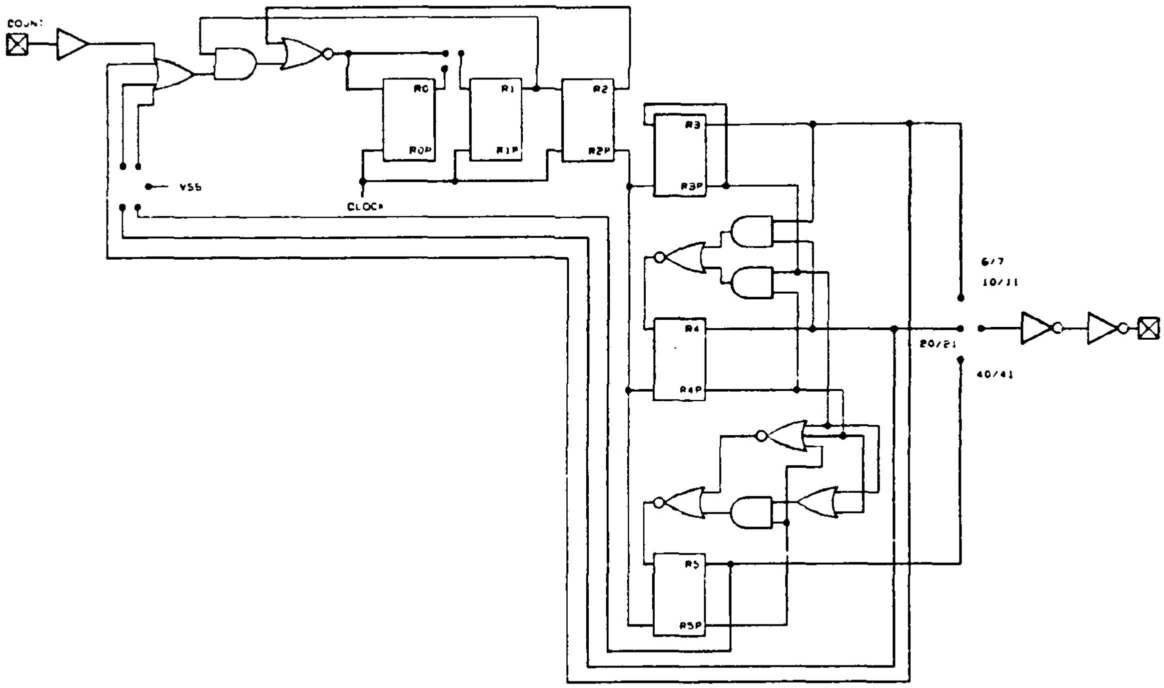


Fig. 2.1-1 Mask programmable prescaler.

Table 2.1-1
Mask Programmable Prescaler Divide Ratios

Prescalar	Divide Ratio
No. 1	6/7
No. 2	10/11
No. 3	20/21
No. 4	40/41

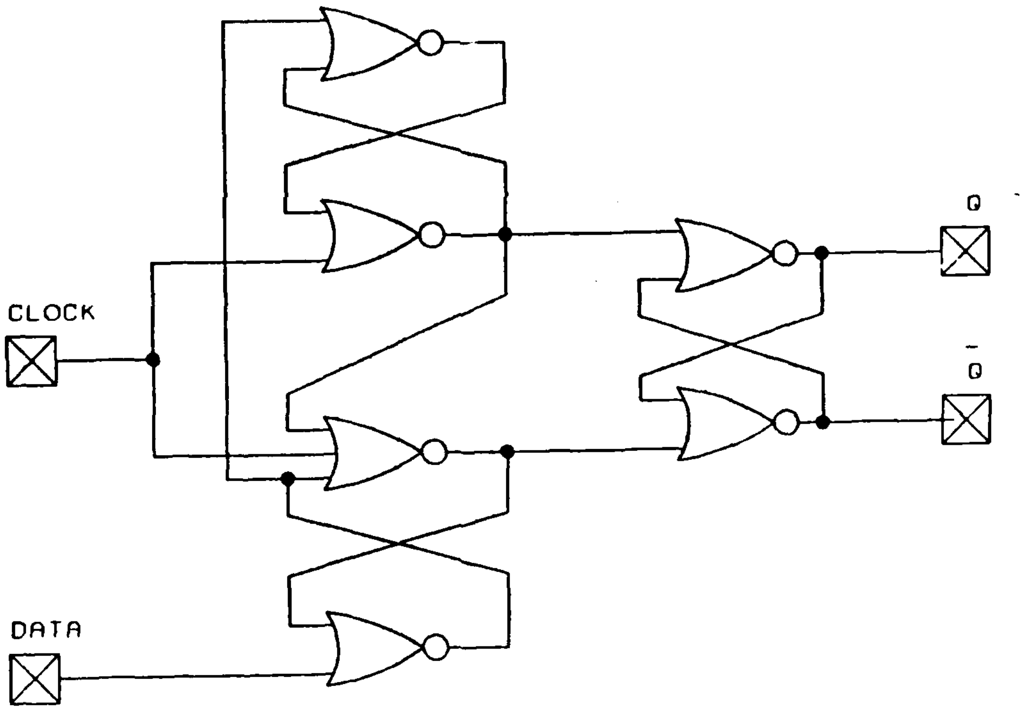


Fig. 2.2-1 Basic flip-flop used in all circuit cells.

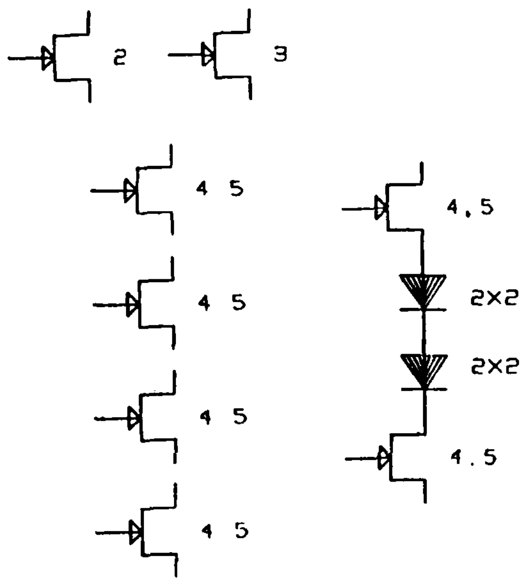


Fig. 2.2-2 Transistor/diode elements used in the SLA.

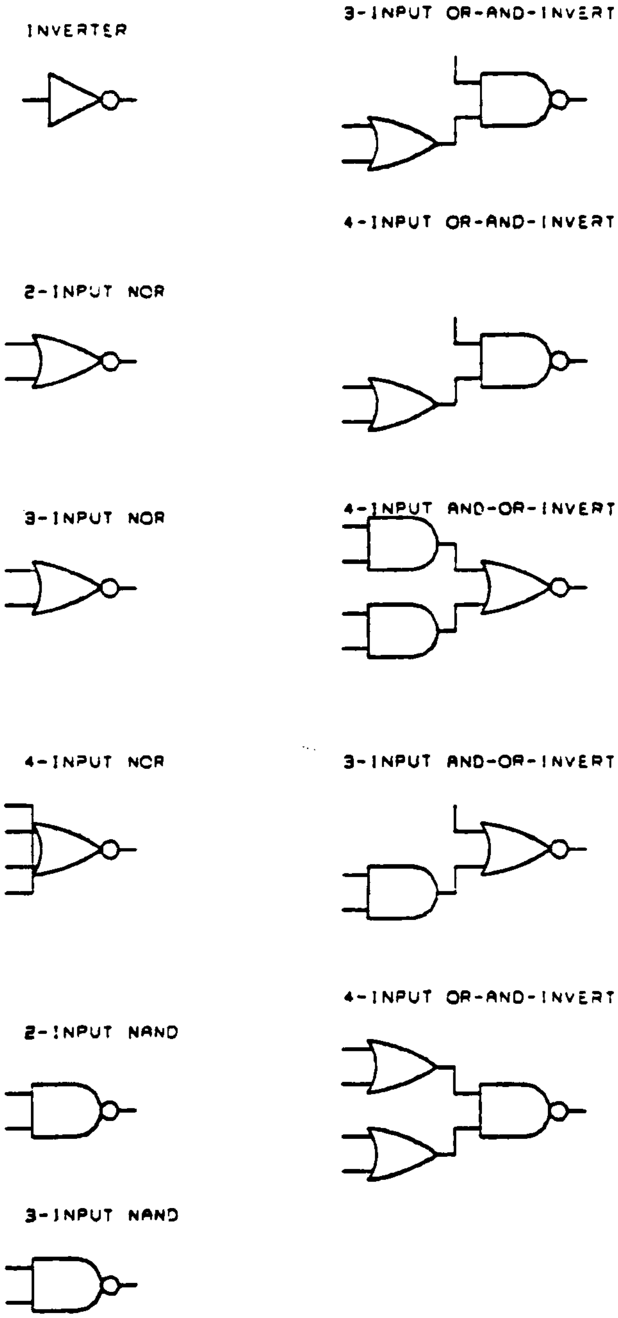


Fig. 2.2-3 Standard gate structures implemented with the transistor/diode elements.

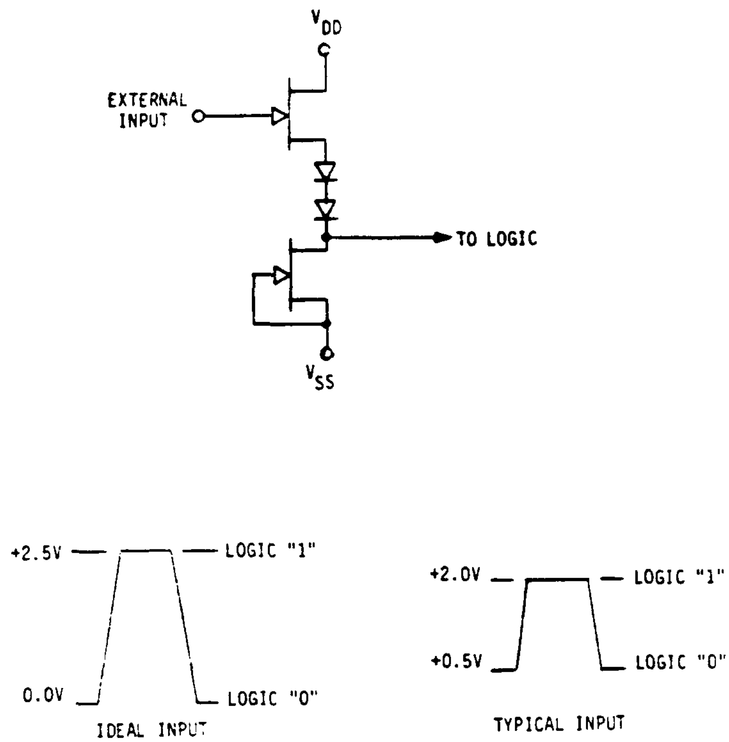


Fig. 2.2-4 Input receiver.

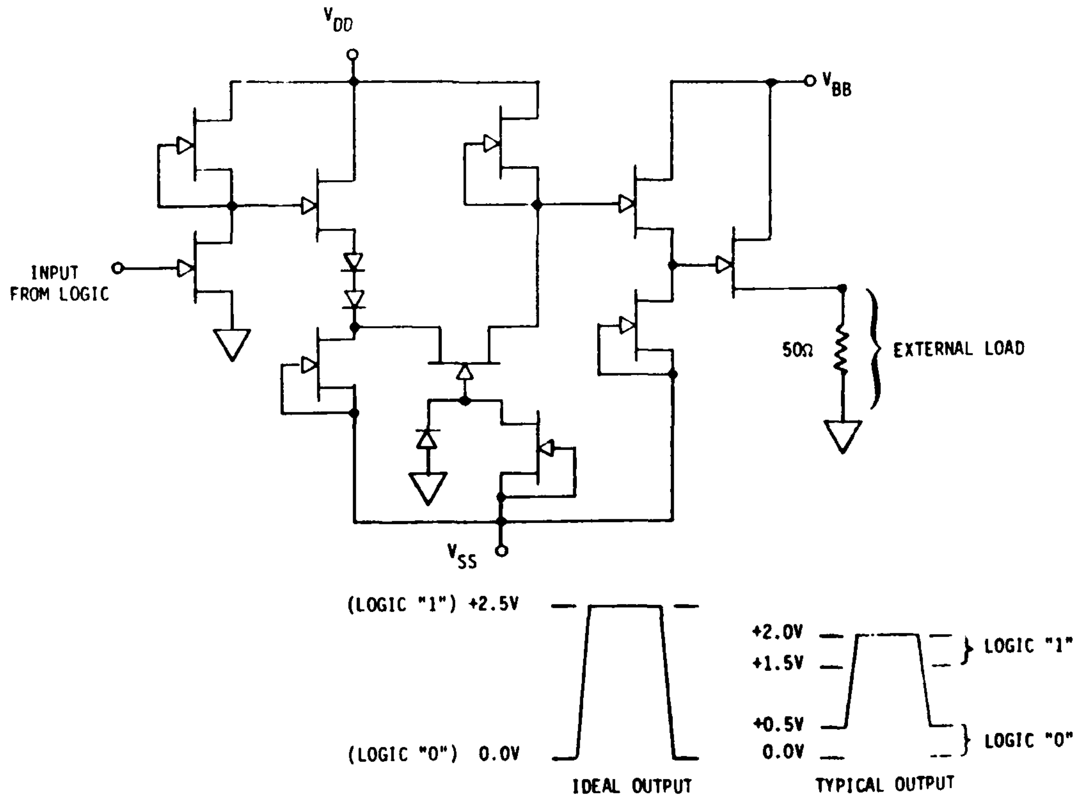


Fig. 2.2-5 Output driver.

2.3 Custom Design

The third design approach used in this program was the custom design of a maximal length pseudo-random sequence generator with 2^{12}-1 bit sequence. The polynomial generated is $G(X) = X^{12} + x^{11} + X^{8} + X^{6} + 1$.

The D flip-flops used for implementing this function were extracted from the storage logic array, and the internal gating required for the feedback connections were custom-designed and placed for optimal circuit performance. Figure 2.3-1 shows a logic diagram of the circuit.

2.4 Parametric and Functional Elements Test Cells

There are 19 test cells included with the ICs as listed in Table 2.4-1.

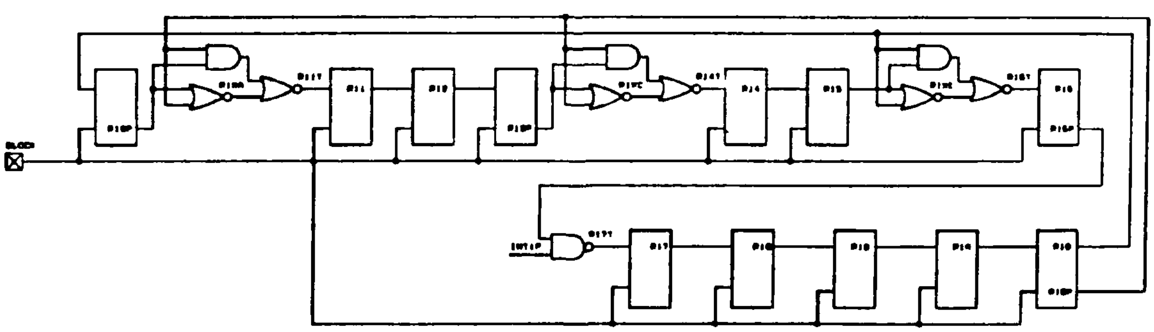


Fig. 2.3-1 Pseudo-random sequence generator.

Table 2.4-1

Test Cells

Cell Number	Function
21	Ring oscillator and divider chain
23, 24, 25, 26	Backgating test structures
27	Horizontal and vertical saturated resistors
28	BFL circuit test device
29, 30, 31	Bidirectional output drivers
32	Memory latch cell
33	Single stage differential receiver
34	Differential amplifier
35	Four-bit counter
36	Divide by 16
37	Crossover test structures
38	Line-to-line and continuity test structures
39	Contact chains
40	Capacitors

2.4.1 Test Cell 21

Cell 21 uses a SLA structure for implementing the ring oscillator and divider circuit. The divider circuit is a series connection of the 12 custom flip-flops and the ring oscillator is structured from the transistor/diode elements.

2.4.2 Test Cells 23, 24, 25 and 26

Cells 23, 24, 25 and 26 form backgating test structures oriented at 0, 45, 90 and 135° angles with respect to the horizontal layout axis. The backgating structures are composed of a single MESFET with a 1 μm gate length and 25 μm wide with nine fingers oriented parallel to the transistor gate and separated from the transistor in 3 μm increments.

2.4.3 Test Cell 27

Cell 27 is a comparative structure composed of five horizontally placed transistors, three horizontally saturated resistors, and three vertically saturated resistors for comparing transistor/resistor characteristics.

2.4.4 Test Cell 28

Cell 28 is a GaAs test structured for buffered FET logic (BFL) circuits. It performs the OR-AND invert logic function. However, all circuit elements can be tested as single or double series structures as in the case of the diode and transistor pairs.

2.4.5 Test Cells 29, 30 and 31

Cells 29, 30 and 31 form bidirectional output drivers using different design approaches, which are capable of driving 50 Ω loads. Cell 29 driver is designed with vertically oriented saturated resistors. Cell 30 is an equivalent output driver with horizontally saturated resistors. Cell 31 is also an equivalent (to Cells 29 and 30), except the design is structured with all MESFETs.

2.4.6 Test Cell 32

Cell 32 is a basic storage element (memory latch) incorporating all necessary peripheral circuitry to read or write into the cell.

2.4.7 Test Cell 33

Cell 33 is a single-stage differential receiver used in applications where an input signal to the chip can be amplified to produce a signal and its complement for internal circuit applications.

2.4.8 Test Cell 34

Cell 34 is a differential amplifier used in applications for signal reconditioning or voltage comparator functions.

2.4.9 Test Cells 35 and 36

Cells 35 and 36 are standard test structures used in the GaAs processing facility for parametric measurements, as well as for engineering device evaluation.

2.4.10 Test Cells 37, 38, 39 and 40

Cells 37, 38, 39 and 40 are parametric test structures designed to monitor etching resolution, metal continuity, vias and insulator integrity. Cell 37 is an orthogonal network of conductors composed of first and second level metal conductors. Cell 38 is a metal line-to-line (etching resolution) and continuity test structure. The metal lines are etched with different separations to determine process resolution. Pads are placed at the beginning and end of each metal run to determine continuity for various widths of conductors. Cell 39 is a contact chain test structure composed of first and second level metal with via interconnects. Cell 40 is a capacitor test structure composed of the various conductive layers (i.e., N^+ metal 1, metal 2) with nitride/oxide dielectrics.

3.0 WAFER PROCESSING

Three wafer lots, of four lots each, were processed for this project and wafer identification was established, as shown in Table 3.0-1.

Table 3.0-1
Wafer Identification

Processing Number	Lot No. 1	Lot No. 2	Lot No. 3
JE1-*	11	21	31
JE1-*	12	22	32
JE1-*	13	23	33
JE1-*	14	24	34

* Lot and wafer number

The general processing steps for the BFL depletio ı-mode technology as used for the circuits is shown in Fig. 3.0-1.

Circuit test data, as reported in this document, was obtained from wafers JE1-11 and JE1-14 of wafer Lot 1. Parametric data was taken from all processed wafers. However, the parametric data included in this report will cover only the wafers which were tested for functional circuits. Although parametric data was taken on all wafers processed, wafer Lot 2 was scrapped due to photoresist adhesion problems during the Schottky metalization step which caused bridging within the circuit elements.

3.1 Parametric Test Data

The parametric test data, taken after completion of wafer processing, includes the following information.

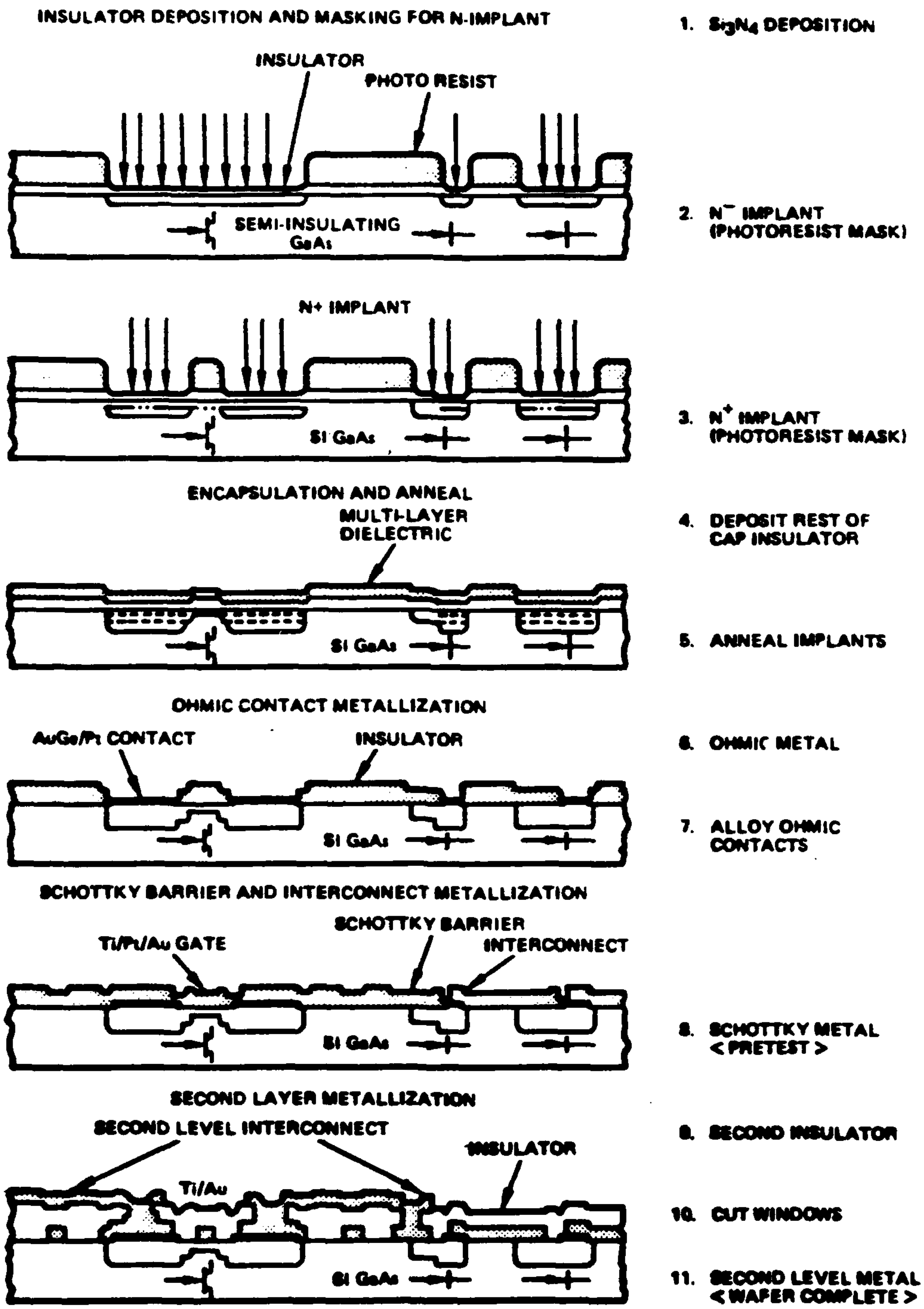


Fig. 3.0-1 Planar GaAs IC fabrication steps.

Transistor (1 μm Gate Length - 50 μm Wide)

V_P - Pinchoff voltage. Calculated from I_{DSS} vs V_{gs} measurements

I_{DSS} - Drain Current. Measured with zero gate bias and V_{DD} = +2.5 V

ID_{SS} V_S V_P - Plot of transistor characteristics with V_{DD} = +2.5 V

Logic Diode (2 μm Wide)

V_B - Barrier height. Calculated from device measurements and processing materials.

V_σ - Voltage drop. Forward voltage drop across diode measured at 150 μA current level

RS - Diode resistance. Extracted from linear portion of forward conductance I-V curve

Figures 3.1-1 through 3.1-6 show the test data on wafer JE1-11, and Figs. 3.1-7 through 3.1-12 show the same data format for wafer JE1-14 which was proton-bombarded to reduce backgating effects.

The processing goal for transistor pinchoff voltage was -1 V ± 10%. The wafers selected for testing had V_P's of -0.92 V and -1.05 V, with standard deviations of 10.5% and 5.6%, respectively.

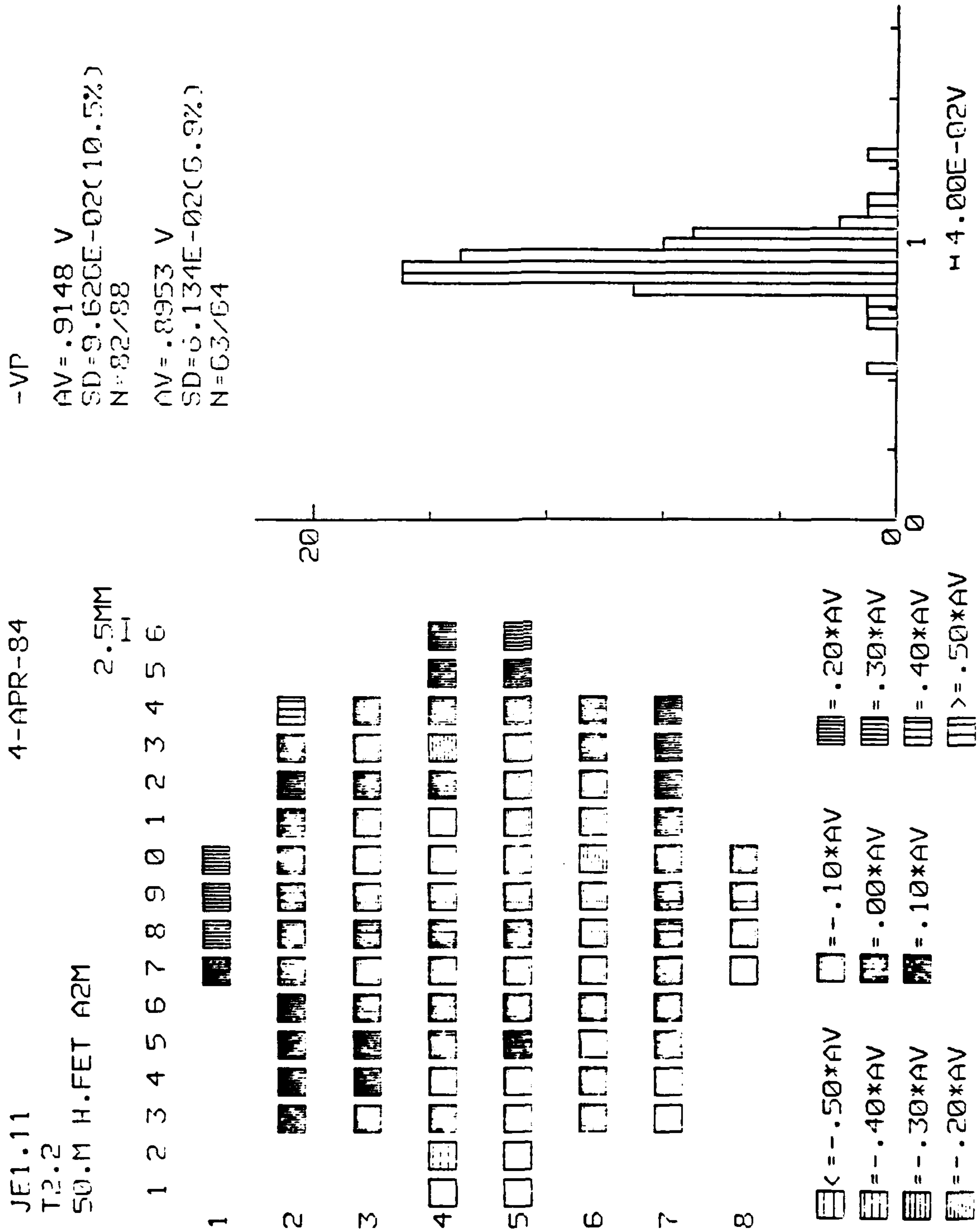


Fig. 3.1-1 Pinchoff voltage.

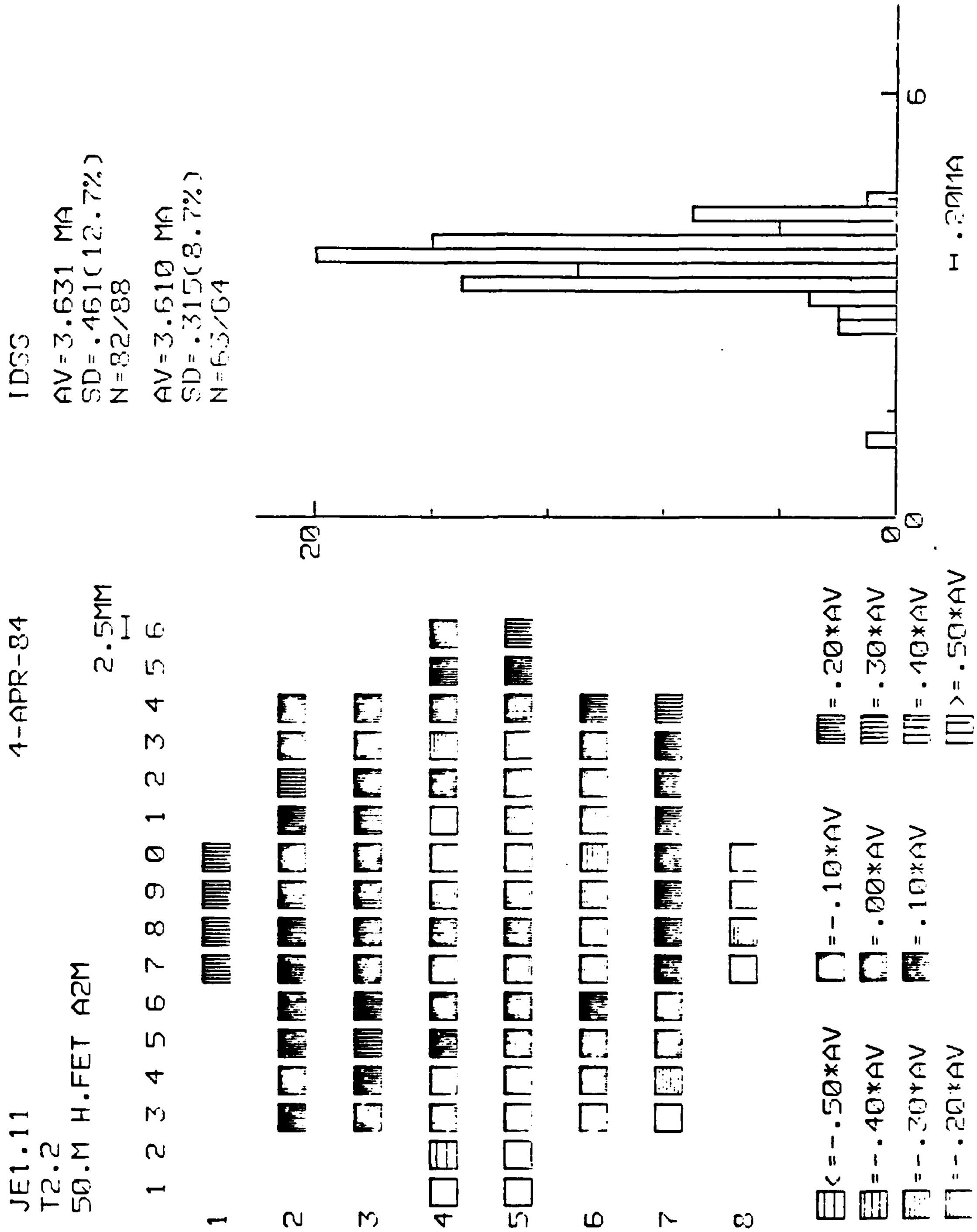


Fig. 3.1-2 Drain current.

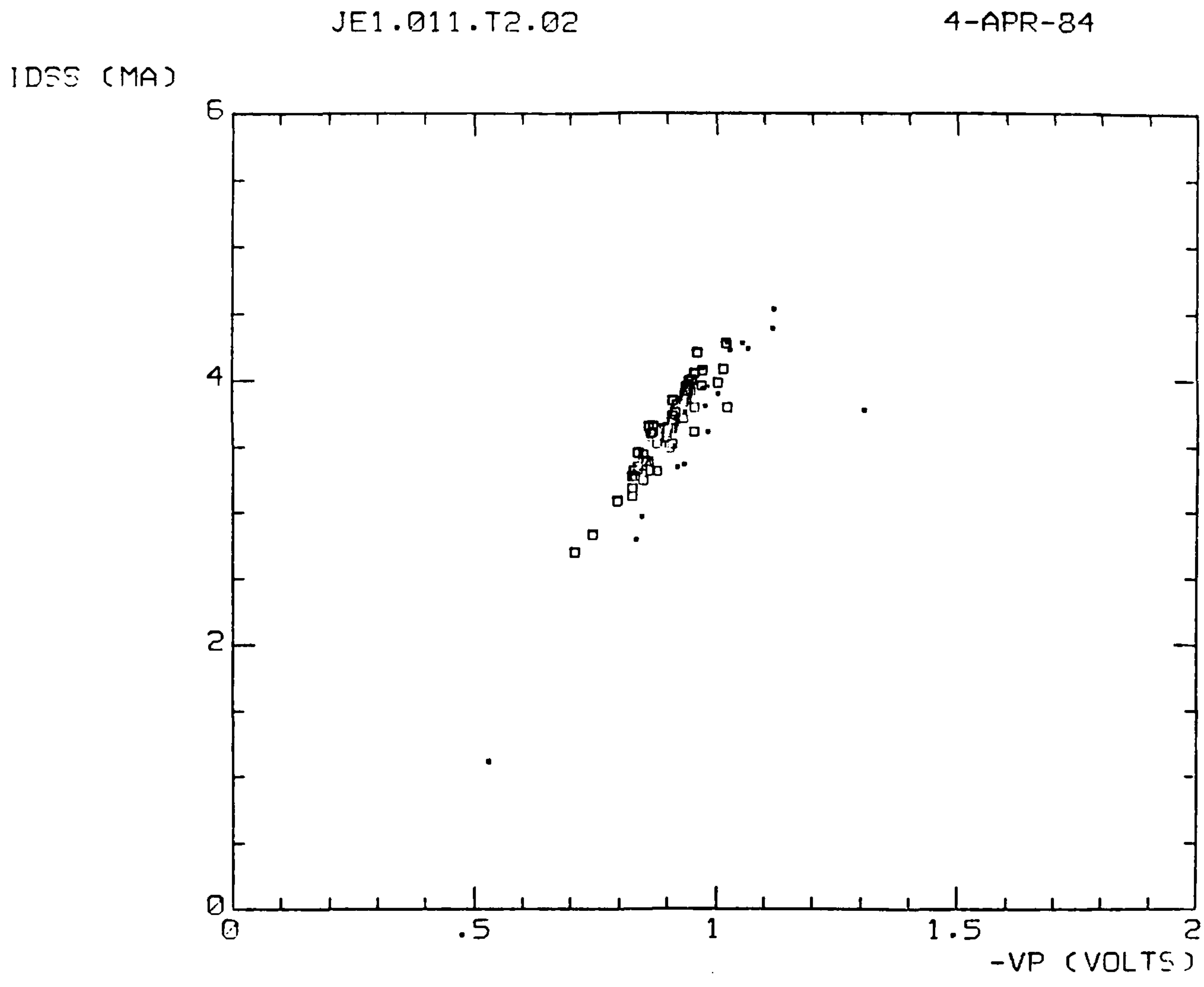


Fig. 3.1-3 I_{DSS} vs V_p.

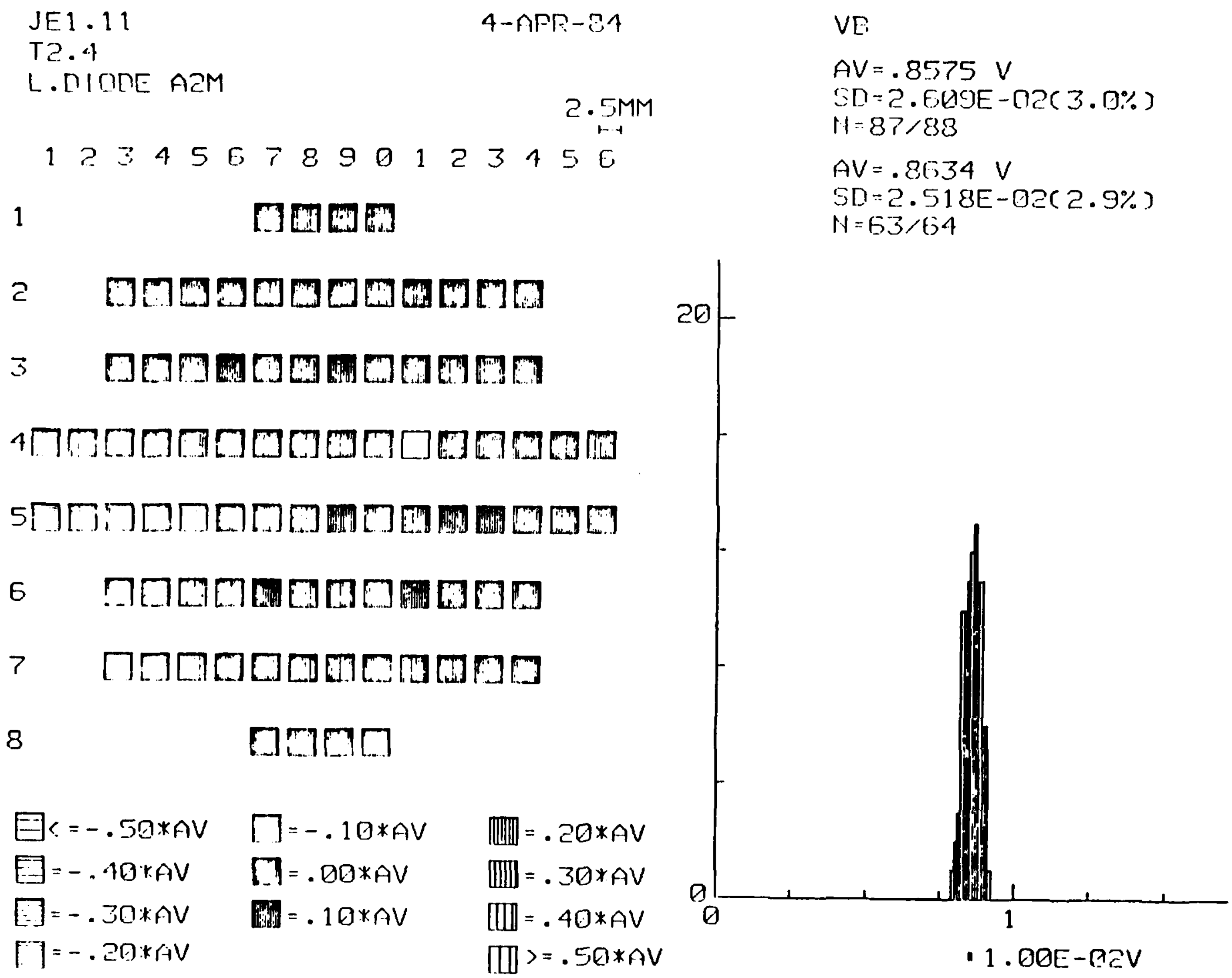


Fig. 3.1-4 Diode barrier height.

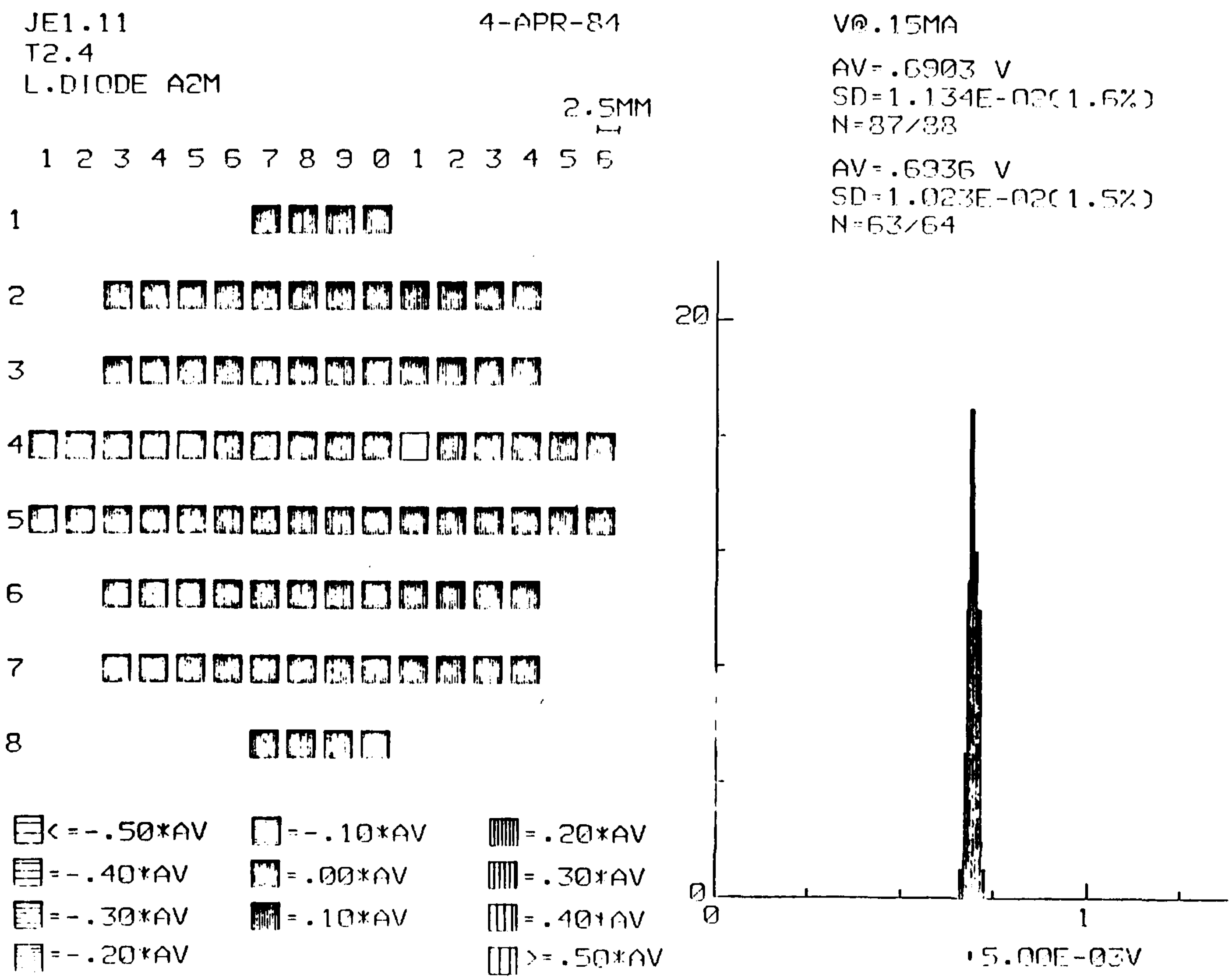


Fig. 3.1-5 Diode forward voltage drop.

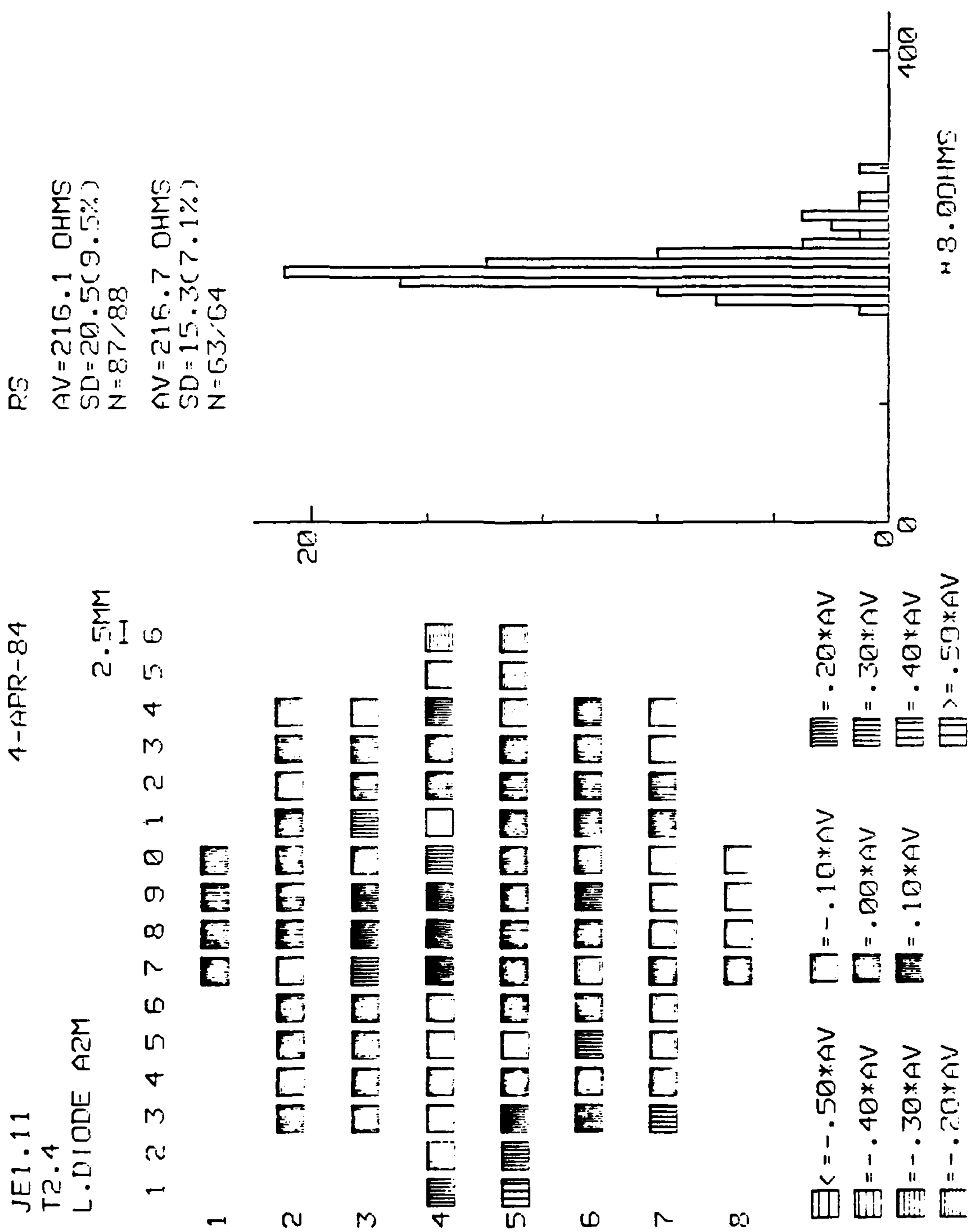


Fig. 3.1-6 Diode resistance.

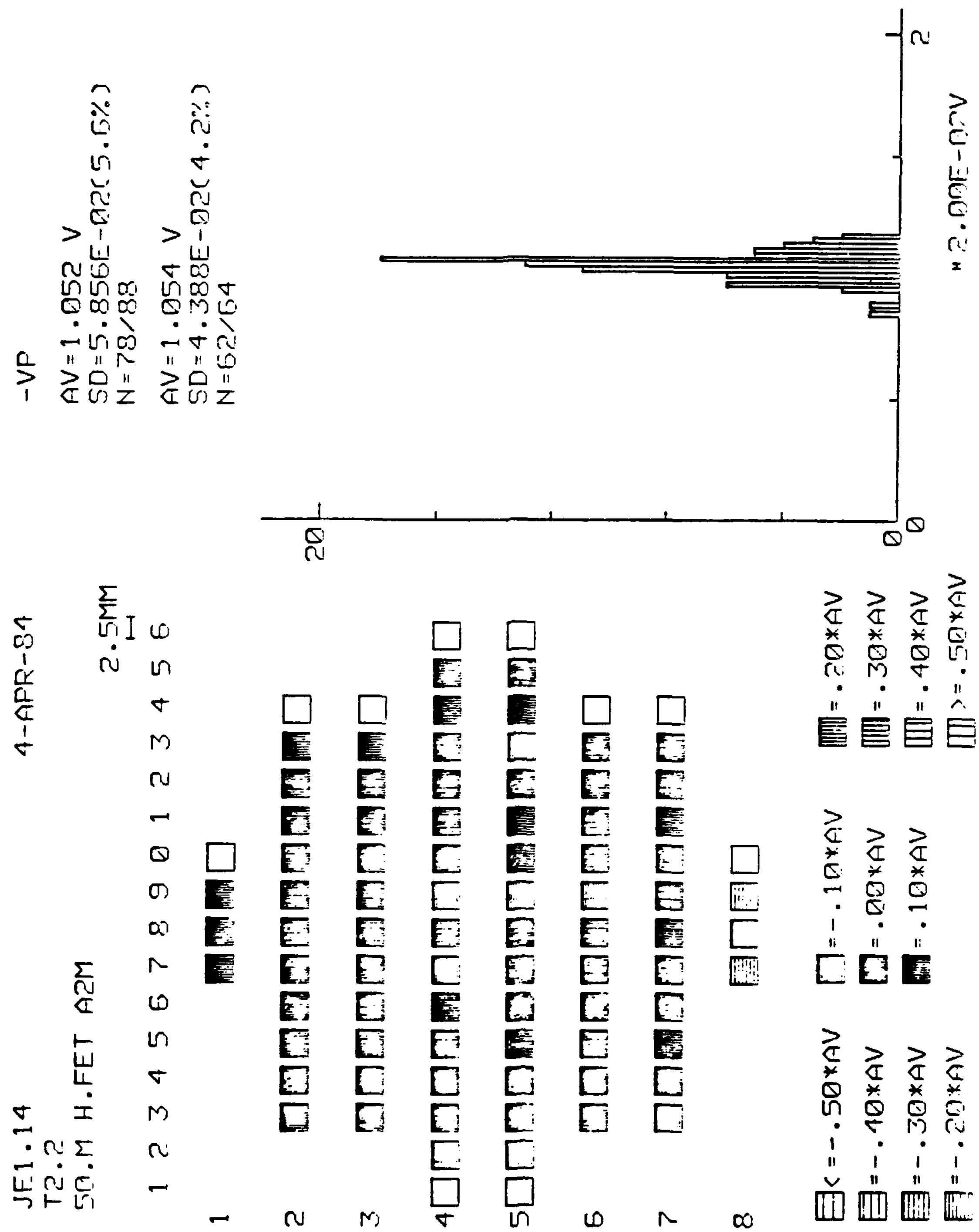


Fig. 3.1-7 Pinchoff voltage.

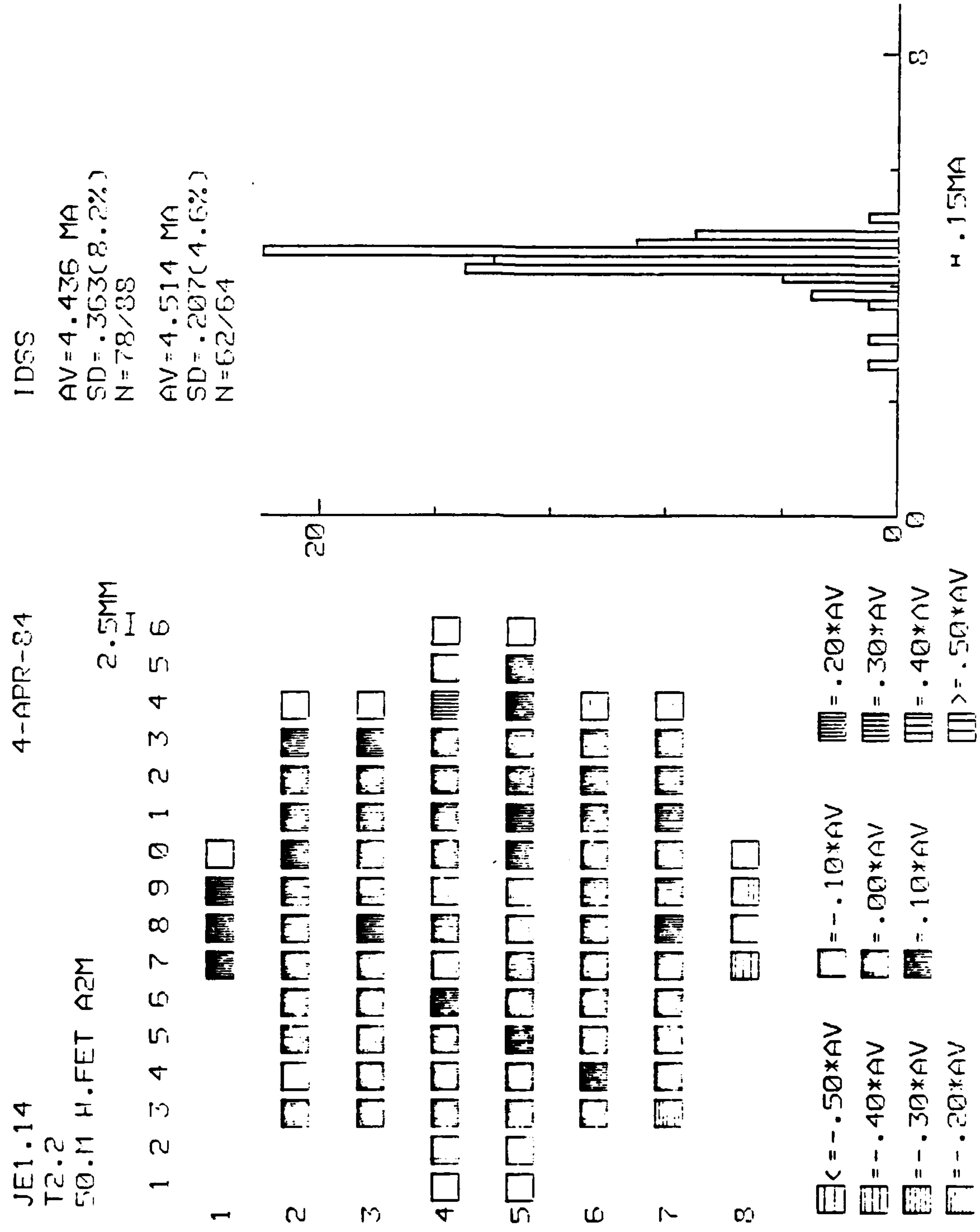


Fig. 3.1-8 Drain current.

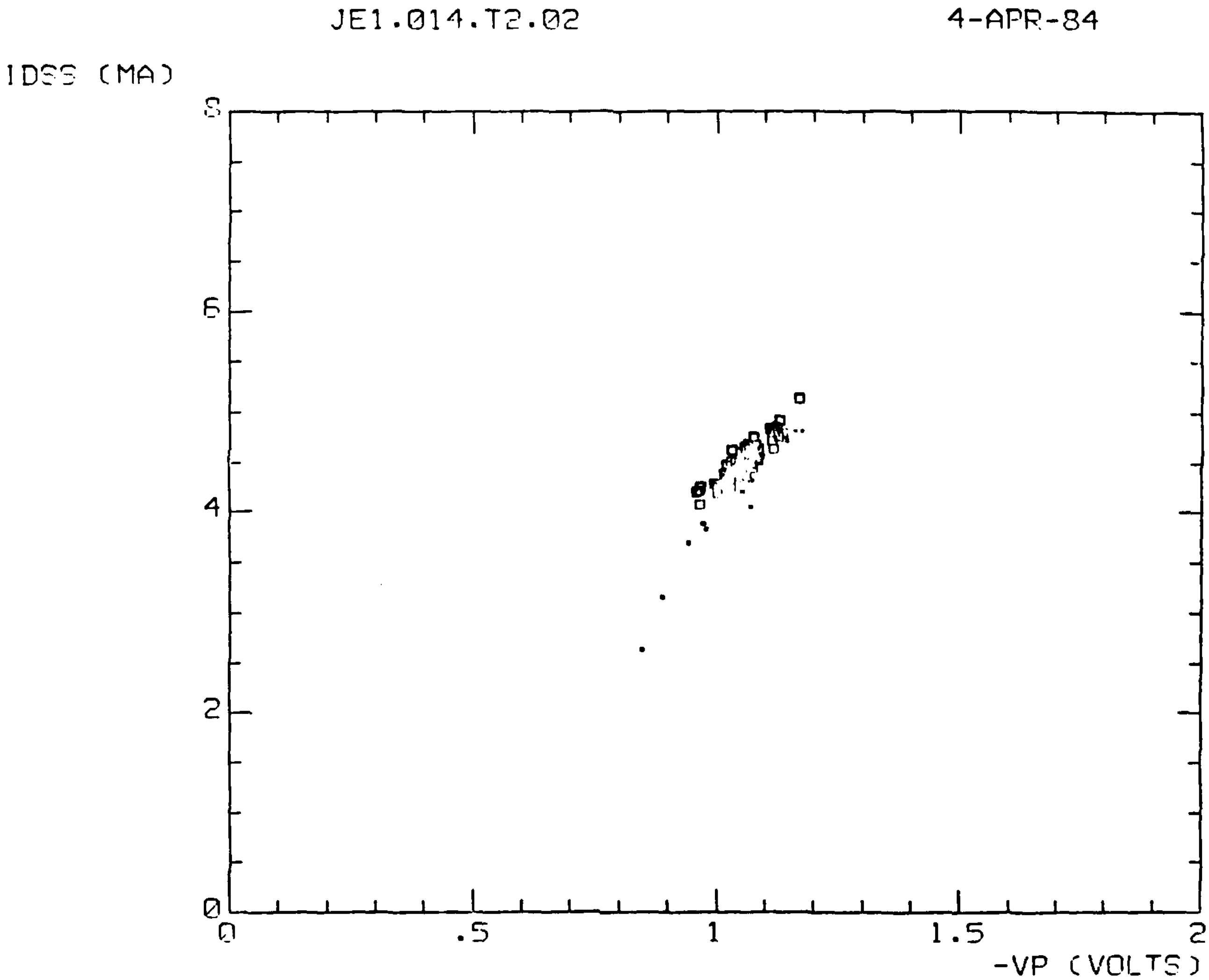


Fig. 3.1-9 I_{DSS} vs V_P.

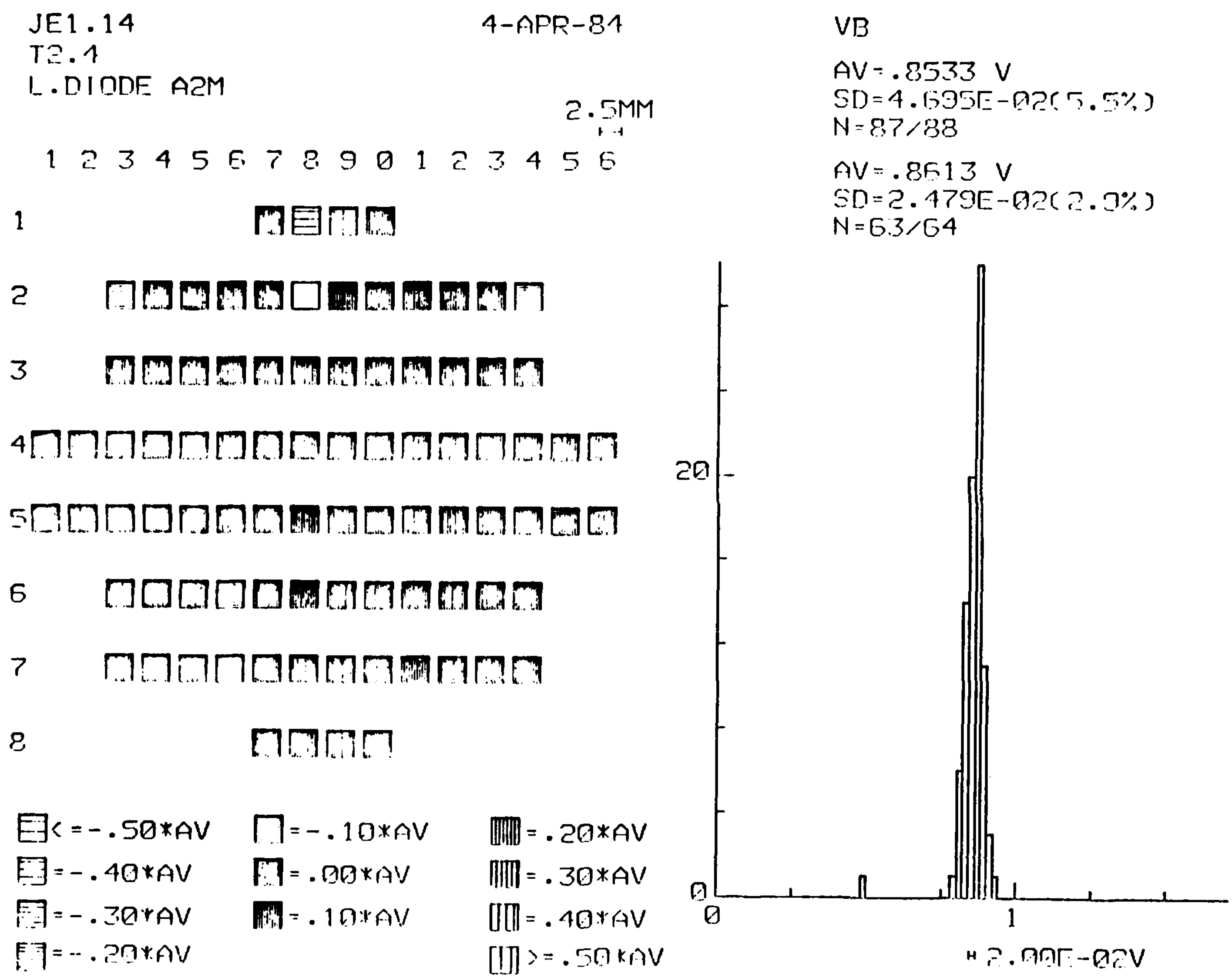


Fig. 3.1-10 Diode barrier height.

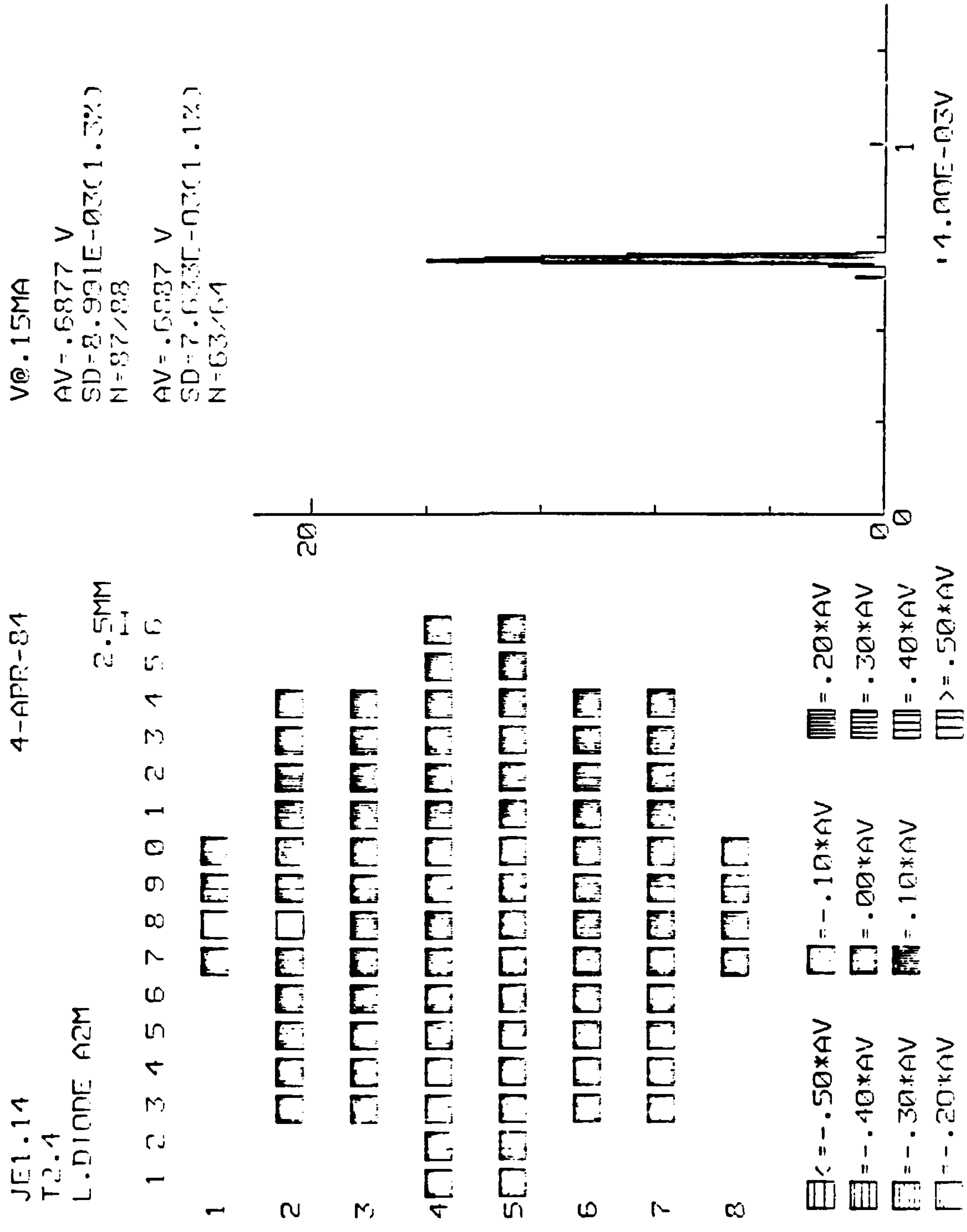


Fig. 3.1-11 Diode forward voltage drop.

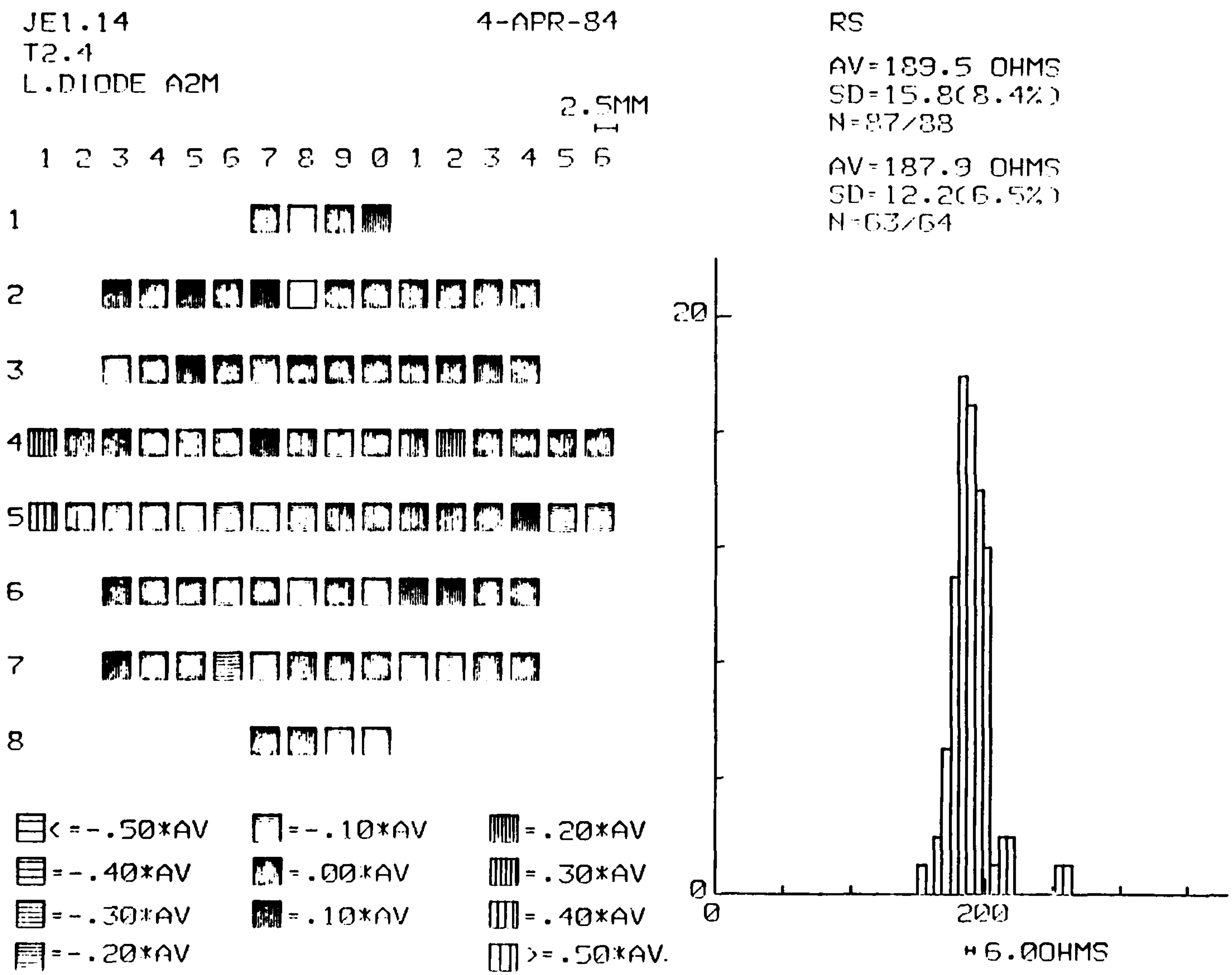


Fig. 3.1-12 Diode resistance.

4.0 MACRO DIE DESCRIPTION AND DEVICE TEST DATA

A top-down CALMA plot of the Phase IIA macro die, including all circuit and test cells, is shown in Fig. 4.0-1. The circuit cells are identified by number and listed in Table 4.0-1 as to the function performed by each cell nd the circuit implementation technique used.

In addition to the circuit cells, there are 19 test cells contained within the macro die, as listed in Table 4.0-2.

All circuits and some test cells were tested for speed and operational characteristics and will be fully reported in the following sections. Preliminary device testing (low speed wafer probe) indicated no design errors in the circuit elements. Testing at wafer probe and packaged devices was performed at room temperature (~ 25°C); therefore, we have no environmental data to report.

Due to the massive number of circuit elements to be tested, we concentrated our final test efforts on devices to be delivered which included the mask programmable prescaler and the SLA accumulators.

4.1 Test Data on Circuit Elements

As mentioned in Sec. 4.0, all circuit elements were tested, at wafer probe, for low frequency operational characteristics and design integrity. These tests were also used to identify circuits to be packaged for high speed testing and to supply yield data as reported in Sec. 5.0.

The circuits were designed to operate at standard voltage levels of V_{DD} = +2.5 V and V_{SS} = -2.0 V. Operational characteristics of the circuit elements, diodes and transistors were slightly different than those used in the models for circuit analysis. Therefore, the V_{DD} supply was adjusted to +2.8 V to compensate for the difference. All test data were obtained at the higher V_{DD} level.

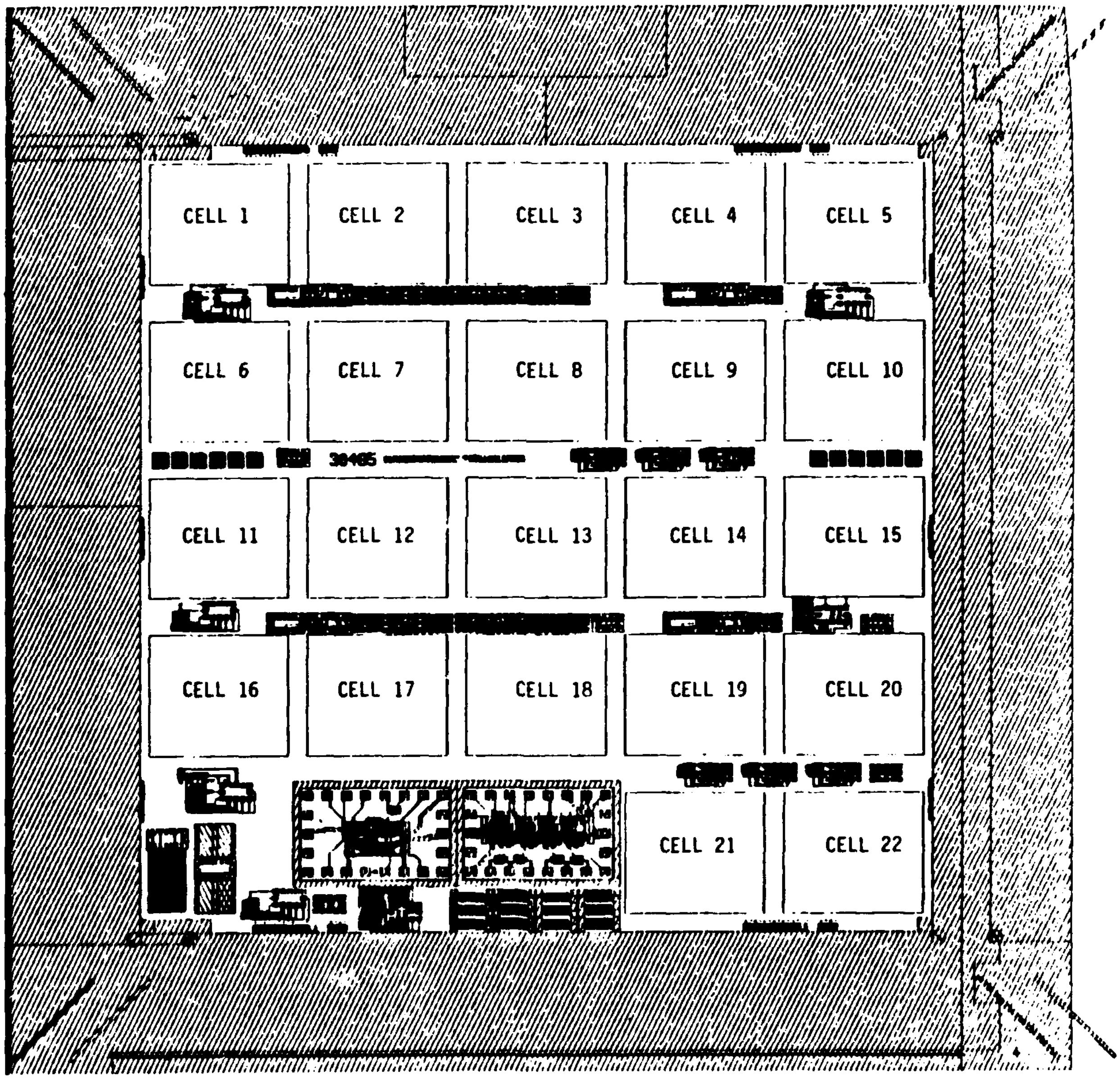


Fig. 4.0-1 Top down CALMA plot of the Phase IIA macro die.

Table 4.0-1

Circuit Cell Functions and Implementation Technique

	Function	Cell Numbers
I.	Mask Programmable	
	Prescaler ÷ 6/7	
	÷ 10/11	
	÷ 20/21	16, 19
	÷ 40/41	
II.	Storage Logic Array	
	4-Bit Up/Down Counter	1, 7, 10, 12, 20
	4-Bit Accumulator	3, 9, 11, 18
	4-Bit Universal Shift Register	2, 13
	Types I and II Phase Detectors	4, 6, 15, 22, 1, 2, 3, 7 9, 10, 11, 12
	Prescalar ÷ 10/11	13, 18, 20
	PRN Sequence Generator	5, 14
III.	Custom Design	
	PRN Sequence Generator	8, 17

Table 4.0-2

Test Cells

Cell Number	Function
21	Ring oscillator and divider chain
23, 24, 25, 26	Backgating test structures
27	Horizontal and vertical saturated resistors
28	BFL circuit test device
29, 30, 31	Bidirectional output drivers
32	Memory latch cell
33	Single stage differential receiver
34	Differential amplifier
35	Four-bit counter
36	Divide by 16
37	Crossover test structures
38	Line-to-line and continuity test structures
39	Contact chains
40	Capacitors

Types I and II phase detectors were tested with very low frequency inputs, and the outputs were monitored to determine performance. This was necessary since they could not be dynamically tested as they would be used in the system. Testing was sufficient to characterize operational characteristics and to prove accurate designs.

4.1.1 Mask Programmable Prescaler

The mask programmable prescalers as listed in Table 4.0-1 were tested to meet the requirements as outlined in Sec. 4.1. All four (6/7, 10/11, 20/21 and 40/41) were operational and performed as required. A logic diagram of the basic circuit is shown in Fig. 4.1.1-1. The count input is designed to control the circuit divide ratio. A logic "0" activates the odd divide ratios of 7, 11, 21 or 41, while a logic "1" gives the even divide ratios of 6, 10, 20 or 40. Programming was accomplished through first level metal, vias and second level metal interconnects.

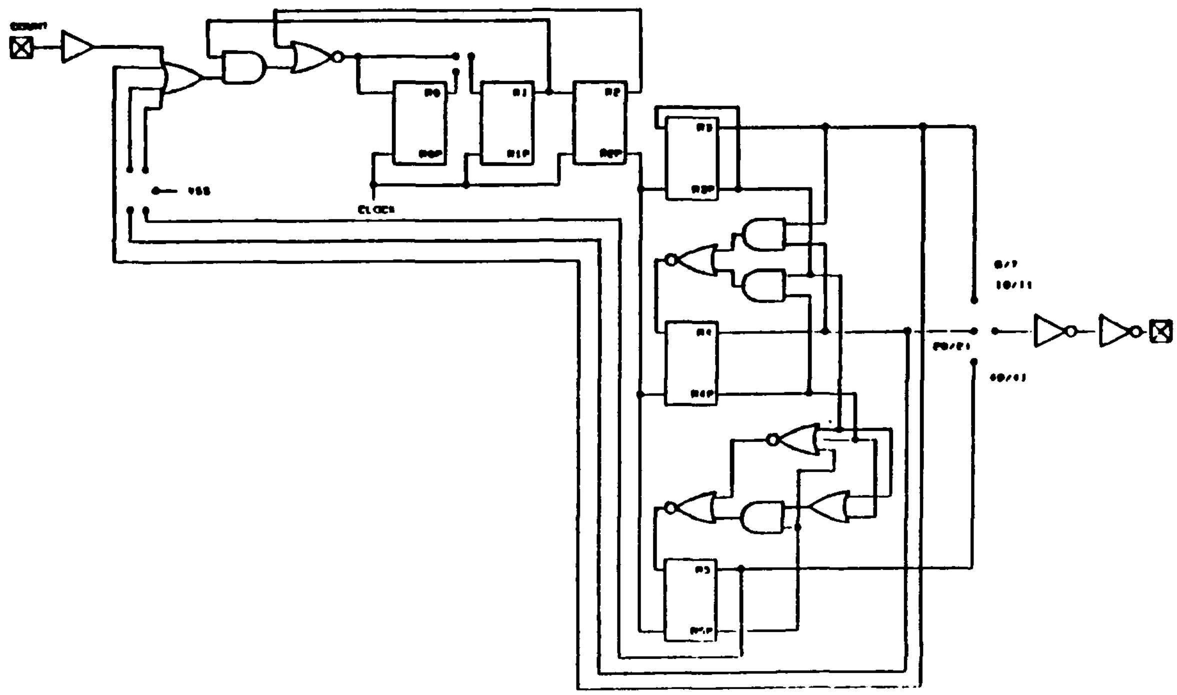
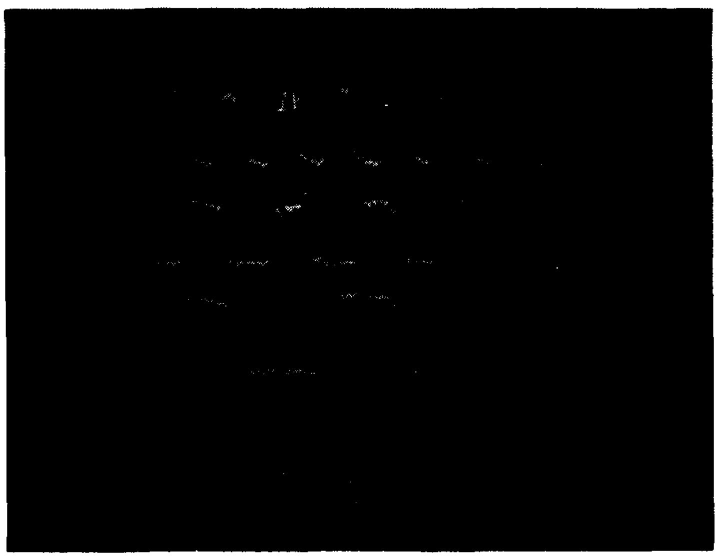


Fig. 4.1.1-1 Programmable prescaler implemented with the mask programmable approach.

Packaged circuits operated with input clock rates up to 1 Ghz; however, a majority of the circuits peaked at 900 MHz. No attempt was made to optimize circuit performance by adjusting the power supplies, since we were concerned about system applications where the supply voltages are fixed.

The output waveforms measured at one cell site are shown in Fig. 4.1.1-2. The test frequency was set at ~ 523 MHz for ease of synchronizing the oscilloscope pattern.

(a) EVEN DIVIDE



(b) ODD DIVIDE

Fig. 4.1.1-2 Output waveforms of mask programmable prescalers (÷ 6/7, 10/11, 20/21 and 40/41) using a 523 MHz clock.

4.1.2 Four-Bit Up/Down Counter

The synchronous 4-bit up/down counter was designed to meet general system applications where various word length requirements could be met by stacking the counters in nibble increments.

A logic design of the counter is shown in Fig. 4.1.2-1. There are eight inputs and five outputs as follows:

Serial input (for stacking)
Control input (S1 and S2)
Parallel input (D0, D1, D2 and D3)
Clock Input

Data outputs (D00, D01, D02 and D03)
Min/Max count output

The function of the control signals is listed in Table 4.1.2-1.

Table 4.1.2-1

Counter Control

Input Control S1	S2	Function
0	0	Parallel load
0	1	Increment
1	0	Decrement
1	1	Hold

A photograph of the output waveforms (excluding D01) is shown in Fig. 4.1.2-2. The clock rate was set to 171 MHz.

4.1.3 Four-Bit Accumulator

An accumulator is an integral component of any direct digital frequency synthesizer where the size (number of bits) is compatible with system performance. For experimental purposes, a 4-bit accumulator was designed to derive performance specifications for application to future communication systems. The accumulator has seven inputs (D0, D1, D2, D3, carry in, clock and reset) and five outputs (E1, E2, E3, E4 and carry out). The carry in and carry out are used to stacking the devices for wide input words.

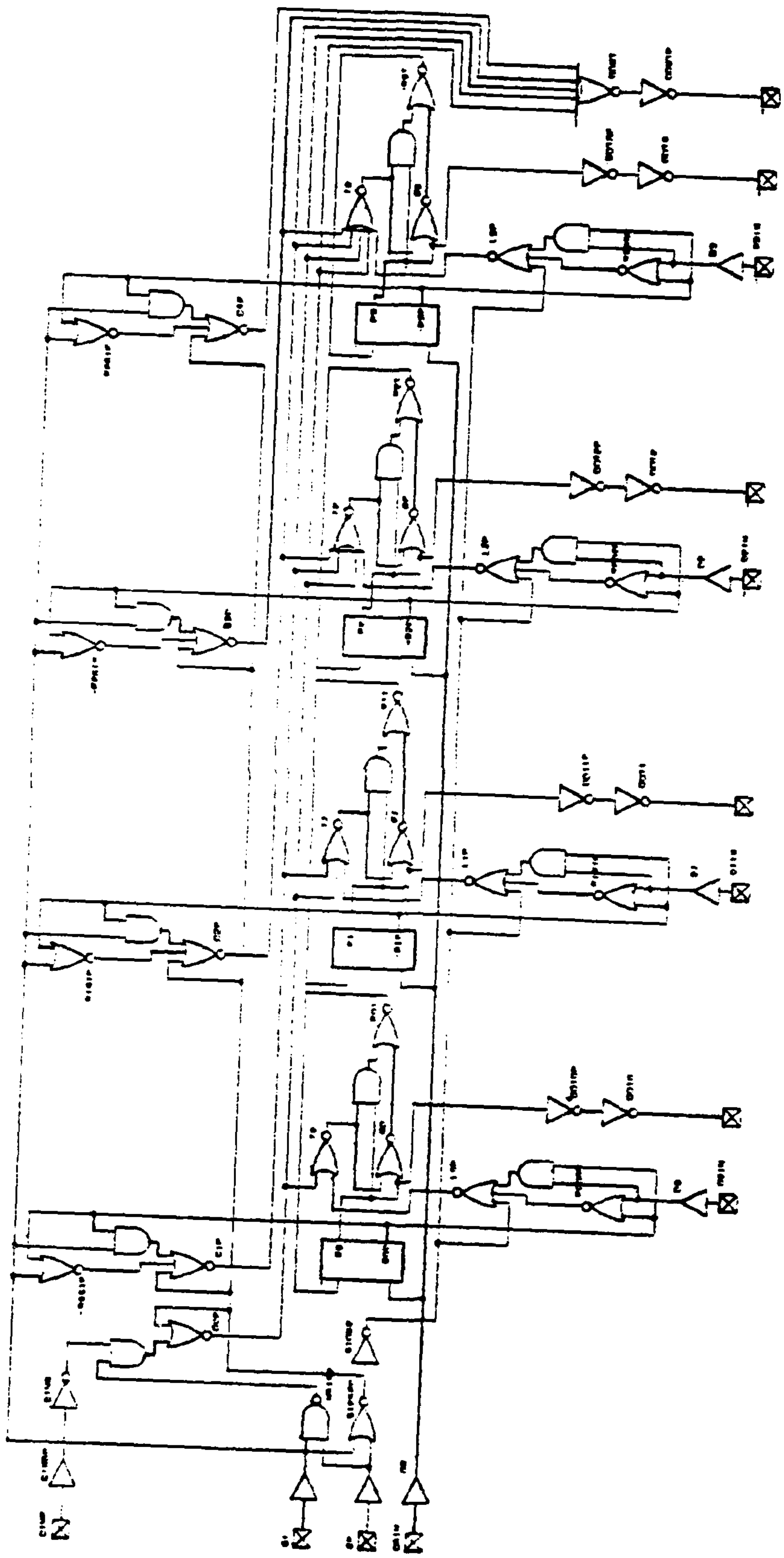


Fig. 4.1.2-1 Four-bit up/down counter with hold and load.

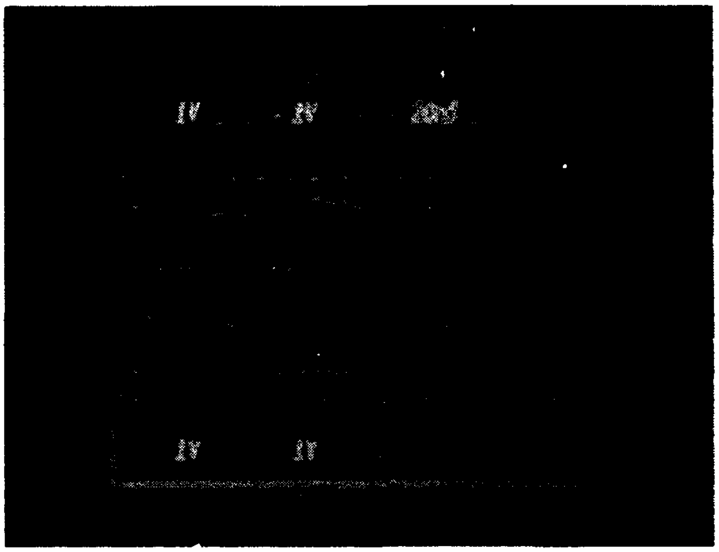


Fig. 4.1.2-2 Output waveforms of the 4-bit up/down counter.

Full operation of the accumulator was obtained at clock frequencies up to 300 MHz. The basic accumulator (without carry out operation) would function up to a clock rate of 410 MHz. The difference indicates a slow path for the generation of the carry out signal.

For systems application with clock speeds of 1 GHz, it is apparent that a 2-bit or possibly a 1-bit accumulator would be required.

A logic diagram of the accumulator is shown in Fig. 4.1.3-1, and the sum outputs of an operational circuit at wafer probe are shown in the oscilloscope display of Fig. 4.1.3-2.

4.1.4 Four-Bit Universal Shift Register

A general-purpose shift register has applications in many system areas, including direct digital frequency synthesizers.

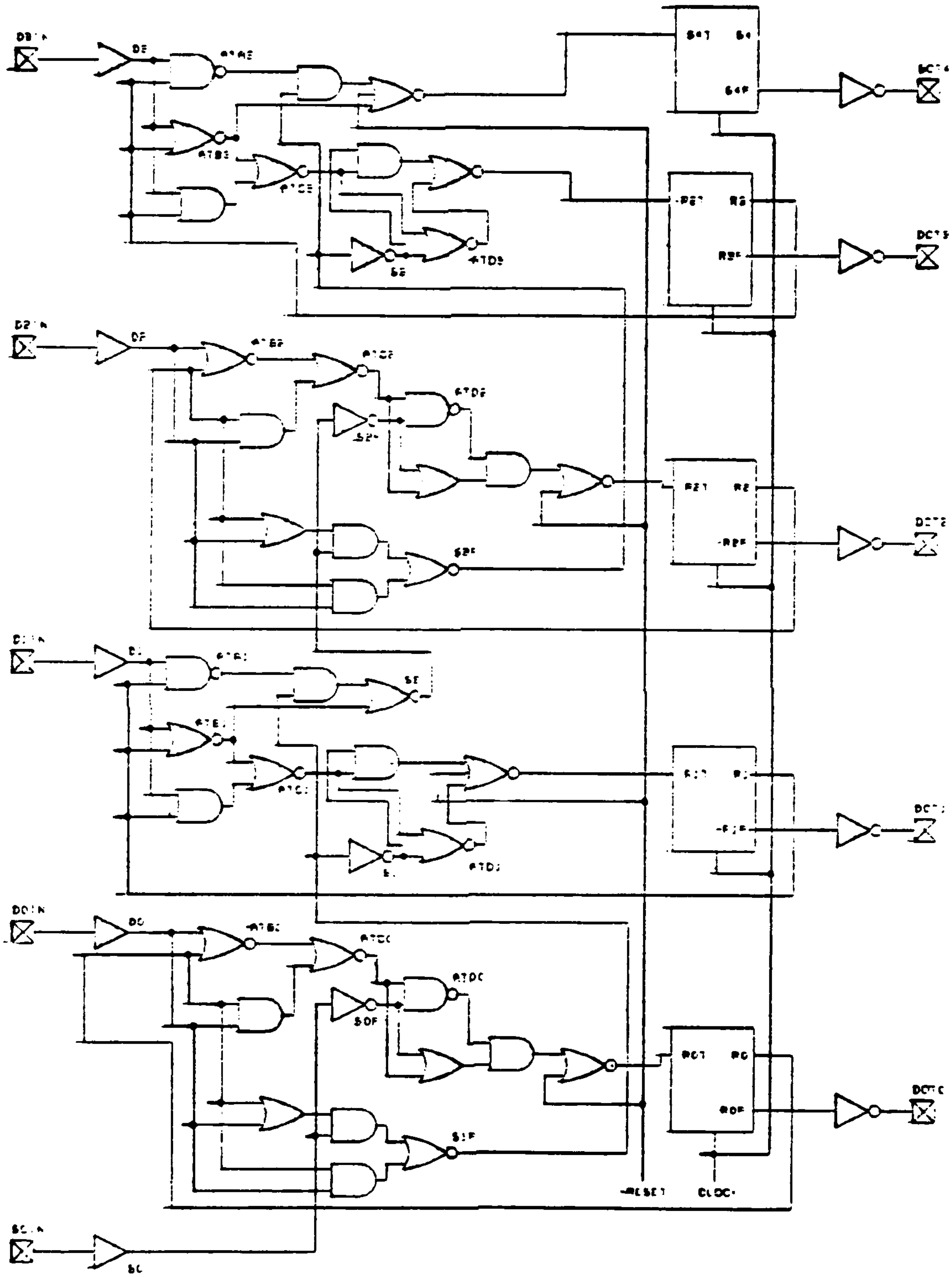
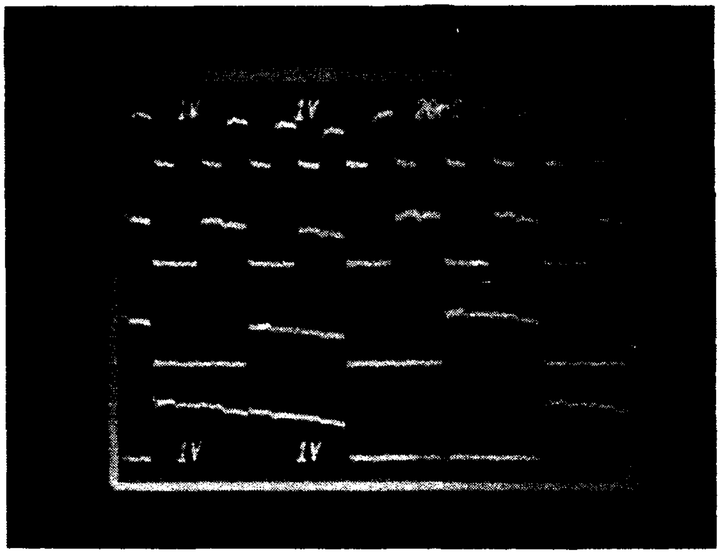


Fig. 4.1.3-1 Four-bit accumulator.



$\Sigma 0$

$\Sigma 1$

$\Sigma 2$

$\Sigma 3$

Fig. 4.1.3-2 Output waveforms (Σ) of the 4-bit accumulator.

The 4-bit universal shift register, designed for this program, goes far beyond the basic design requirements of synthesizer applications. However, it can stand alone as an MSI functional block which has many systems applications.

There are a total of nine input lines and four outputs which include the following:

Parallel inputs (D0, D1, D2 and D3)
Right serial input
Left serial input
Clock input
Control input (S1 and S2)
Outputs (R0, R1, R2 and R3)

A logic diagram of the shift register is shown in Fig. 4.1.4-1. The control lines S1 and S2 control the device, as listed in Table 4.1.4-1.

Table 4.1.4-1

Shift Register Control

Control Lines S1	S2	Decoded Control LS	HD	RS	LD	Function
0	0	0	1	0	0	Hold
1	0	0	0	1	0	Right shift
0	1	1	0	0	0	Left shift
1	1	0	0	0	1	Parallel load

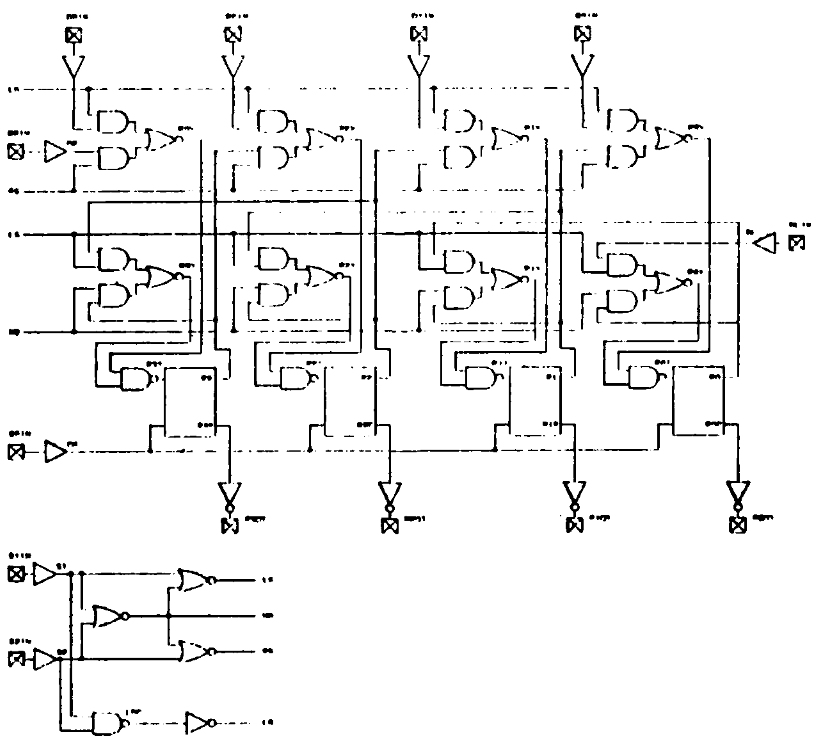


Fig. 4.1.4-1 Four-bit universal shift register.

Operational characteristics of the circuit are shown in Fig. 4.1.4-2, which includes the left and right shift functions at a clock rate of 652.8 MHz. The speed of this circuit is limited by the control networks between the register stages.

4.1.5 Psuedo-Random Sequence Generator

The maximal length pseudo-random sequence generator is composed of 12 flip-flops extracted from a storage logic array and associated logic gates to implement 2^{12}-1 bit sequence which generates the polynomial $G(X) = X^{12} + X^{11} + X^8 + X^6 + 1$. A logic diagram of the circuit is shown in Fig. 4.1.5-1 and the output wave pattern is shown in Fig. 4.1.5-2.

The pseudo-random sequence generator has many applications in communication systems and direct digital frequency synthesizers for masking output spurs associated with fractional division.

To prove correct circuit operation, the output waveform (Fig. 4.1.5-2) was checked against a computer simulation of the circuit. The patterns matched as would be required for a fully functional device.

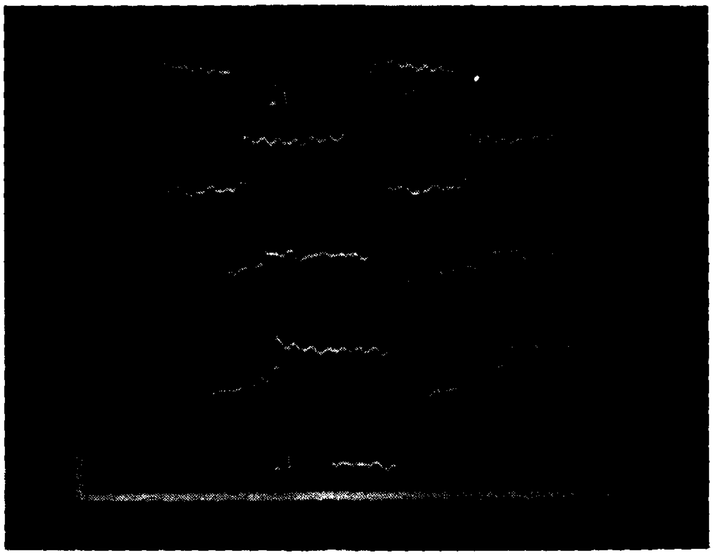
4.2 Wafer Probe Data on Test Devices

Wafer probe test data was taken from the basic test cells, as identified in Table 4.2-1.

Table 4.2-1

Basic Test Cells Tested at Wafer Probe

Cell Number	Function
21	Ring oscillator and divider chain
23	Backgating test structure
28	BFL circuit test device
29,30,31	Bidirectional output drivers
32	Memory latch



(a) RIGHT SHIFT

(b) LEFT SHIFT

Fig. 4.1.4-2 Four-bit universal shift register operating with an input frequency of 46.6 MHz and a clock rate of 652.8 MHz.

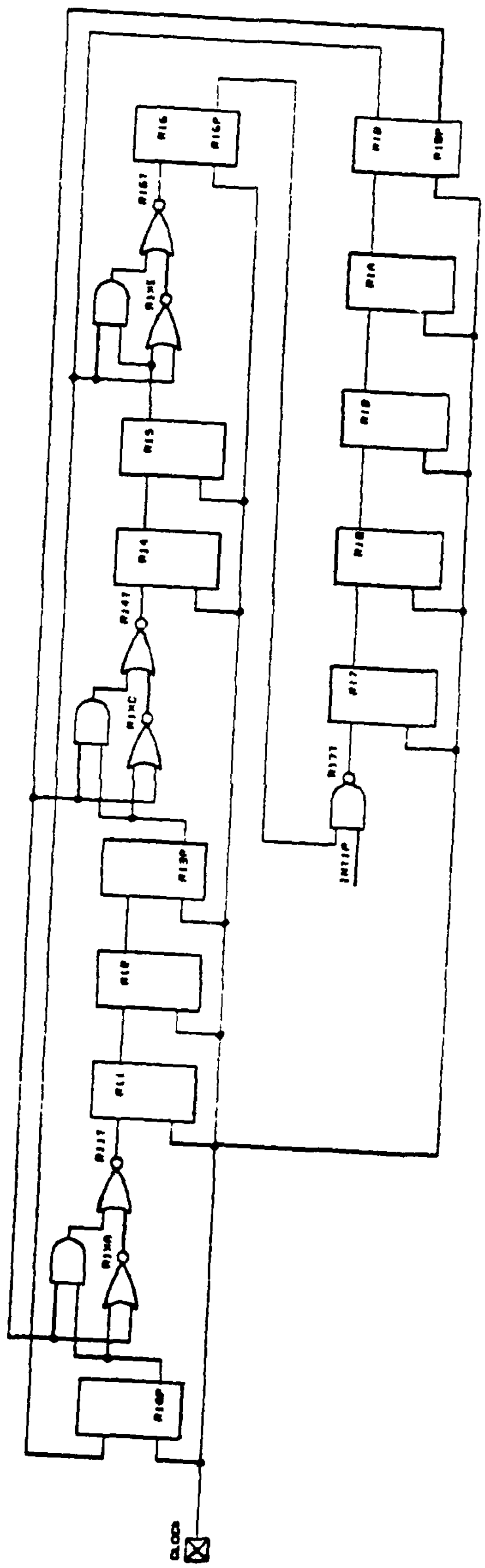


Fig. 4.1.5-1 Pseudo-random sequence generator.

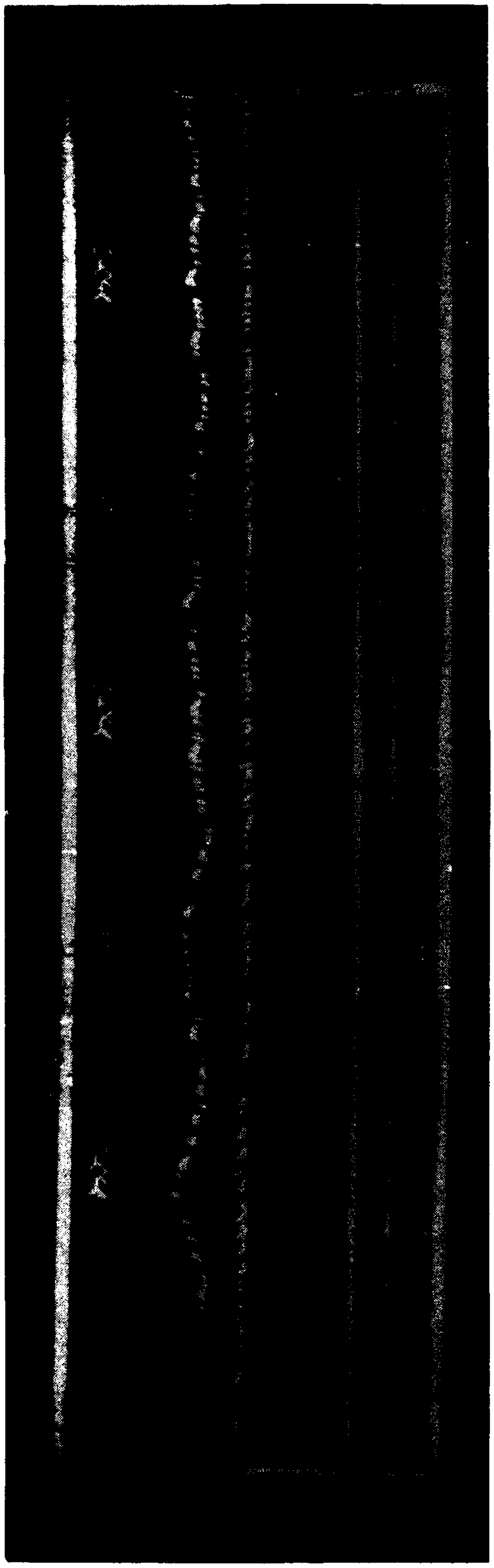


Fig. 4.1.5-2 Pseudo-random sequence generator output.

Although there are many test cells which were not tested, it was deemed unnecessary to continue based on the parametric data derived from the elements, as listed in Table 4.2-1.

4.2.1 Ring Oscillators and Divider Chain

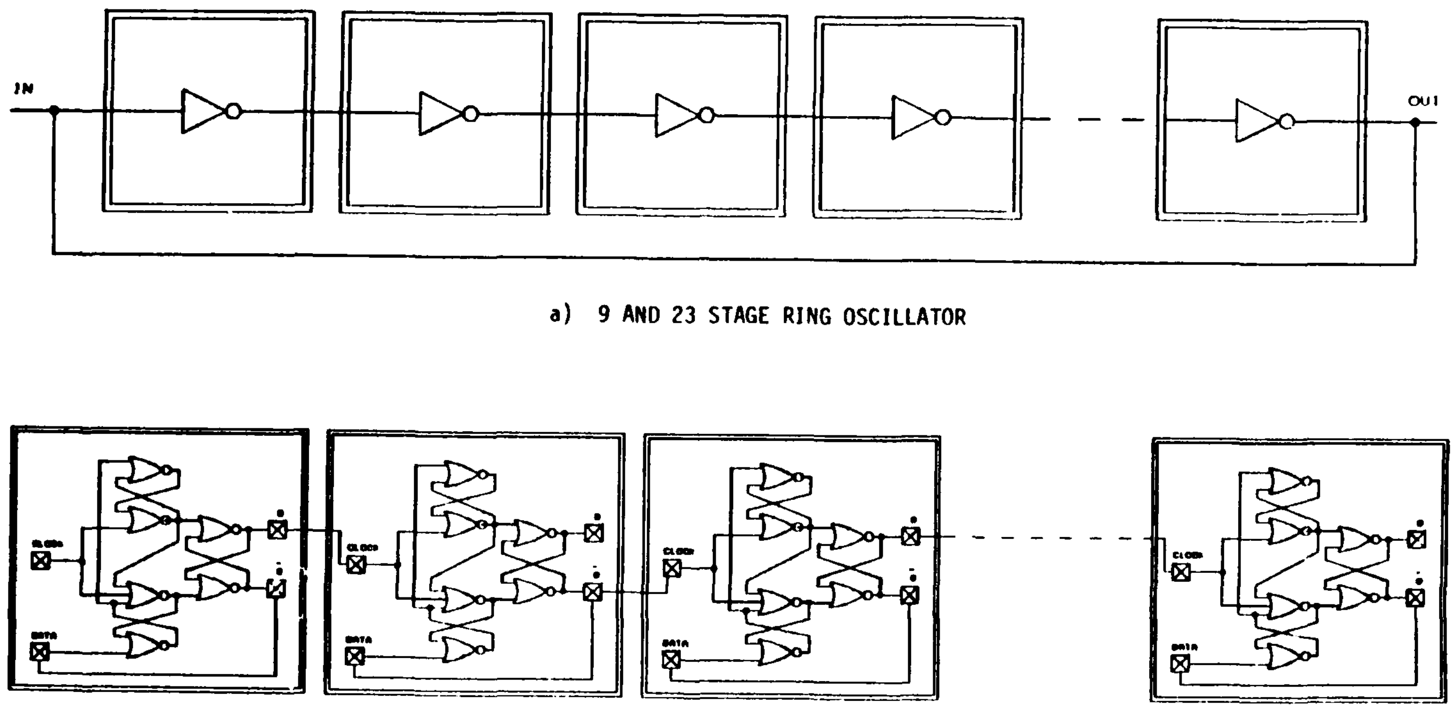
A logic diagram of the inverter stage ring oscillator and flip-flop divider chain circuits is shown in Fig. 4.2.1-1. The ring oscillators were implemented in a storage logic array using the transistor/diode elements to construct the individual inverter stages (Fig. 4.2.1-2) with a fan-in/fan-out of one.

A photograph of the 23-stage oscillator output is shown in Fig. 4.2.1-3, which indicates an output frequency of ~ 114 Mhz, which translates to a stage delay of ~ 190 ps. The range of delay over many test sites was 173 to 195 ps.

Although the speed is high for the small geometry devices used, it does not represent true circuit speed where the logic is constructed of multiple inputs and outputs with a loading factor > 1. What the speed measurement does supply is a reference point for comparison to other unity-loaded ring oscillator data.

To determine the effects of greater circuit loading, an 8-stage NOR gate oscillator was also constructed within the SLA (Fig. 4.2.1-4). The fan-in/fan-out conditions for this circuit was two. Gate delays derived from these tests indicated 275 to 312 ps, which was a 50% increase over the unit-loaded inverter oscillators.

A 12-stage divider (÷ 4096), as shown in Fig. 4.2.1-1, was designed into the SLA using the 12 custom-designed flip-flops contained within the array. The divider operates asynchronously and was to be used to determine maximum speeds of the flip-flops.



a) 9 AND 23 STAGE RING OSCILLATOR

b) 12 STAGE ASYNCHRONOUS DIVIDER CHAIN

Fig. 4.2.1-1 Ring oscillator and divide^ chain.

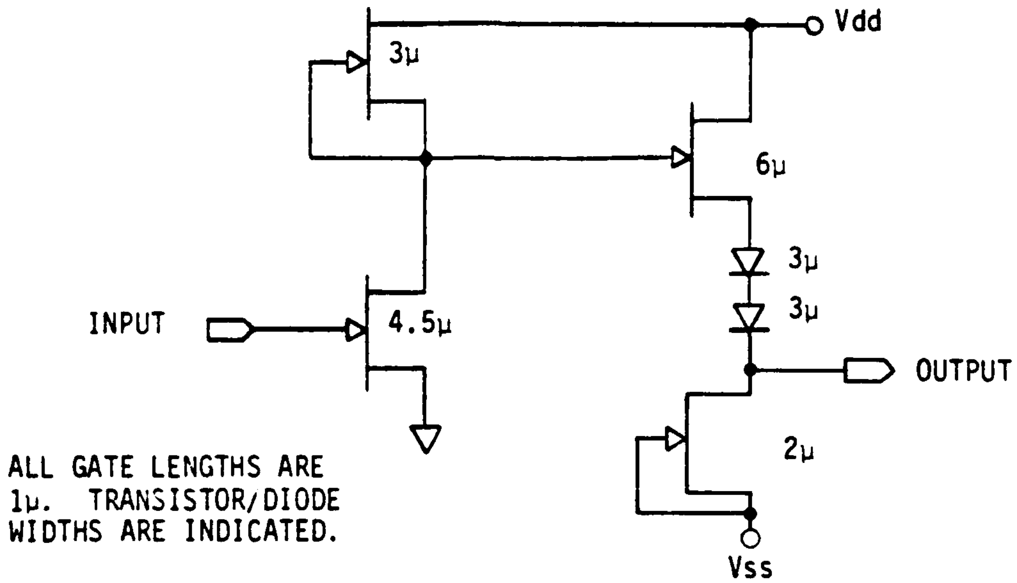


Fig. 4.2.1-2 Inverter stage of ring oscillator.

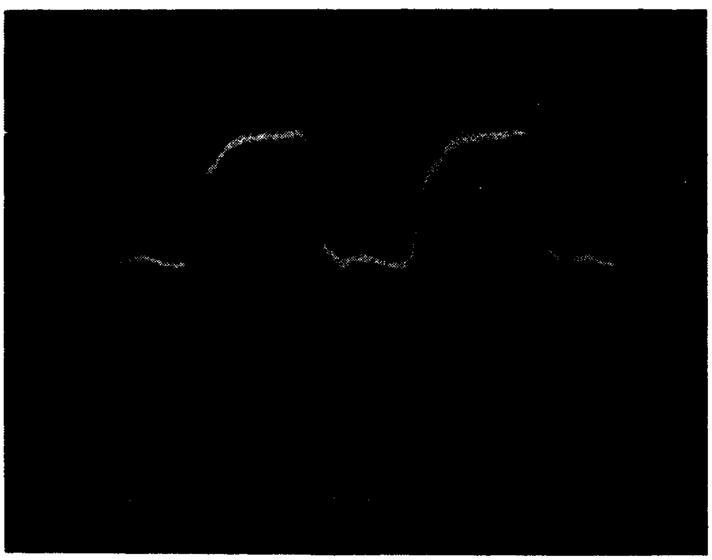


Fig. 4.2.1-3 Ring oscillator output.

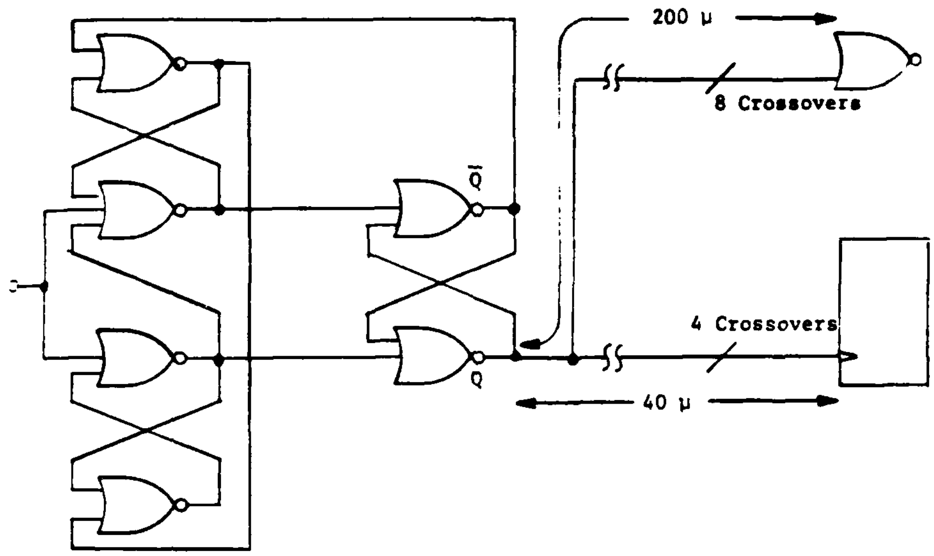


Fig. 4.2.1-4 Eight-stage NOR oscillator.

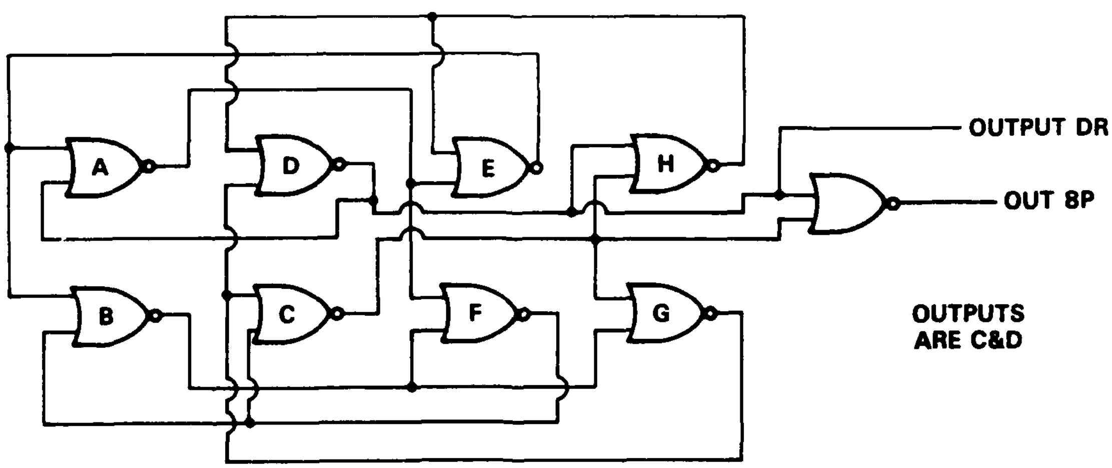


Fig. 4.2.1-5 D flip-flop and loading used in analysis.

Initial wafer probing indicated not operational units at 44 macro die sites. Microprobing of the circuit resulted in the discovery of an open gate on the fifth flip-flop stage source follower. The open gate condition was caused by a particle on the working plate, which was cleaned and examined to prevent the repeated defect on the following wafer lots.

Due to time limitations at the end of the program, no further testing of these elements was performed.

However, there is another approach to estimating the flip-flop speed based on the NOR gate ring oscillator data. The basic NOR gate flip-flop, as shown in Fig. 4.2.2-1, has to total delay through the device for proper setup and hold, such that the maximum operating frequency (toggle rate) is equal to 1/5 γd, where γd is ~ 300 ps.

$$f_{max} = 1/5\ \gamma d = \frac{1 \times 10^{12}}{5\ (300)} \approx 667 \text{ MHz} \quad .$$

Analysis of the flip-flop, as reported on in the Phase I final report, assuming the loading conditions expected to be encountered within the SLA (Fig. 4.2.1-5), predicted a maximum operating speed of 2.5 GHz. Test data from operational circuits indicate a functional frequency > 1 GHz.

4.2.2 Backgating

Four backgating test cells were designed for this project (Sec. 2.4.2, this report). The device selected for collecting the enclosed test data is composed of a horizontal transistor (1 μm gate length and 25 μm wide) with nine backgating fingers placed at incremental steps of 3 μm from the transistor, as shown in Fig. 4.2.2-1.

To perform the test, the transistor was connected to operate as either a pull-up or switching transistor, as depicted in Fig. 4.2.2-2.

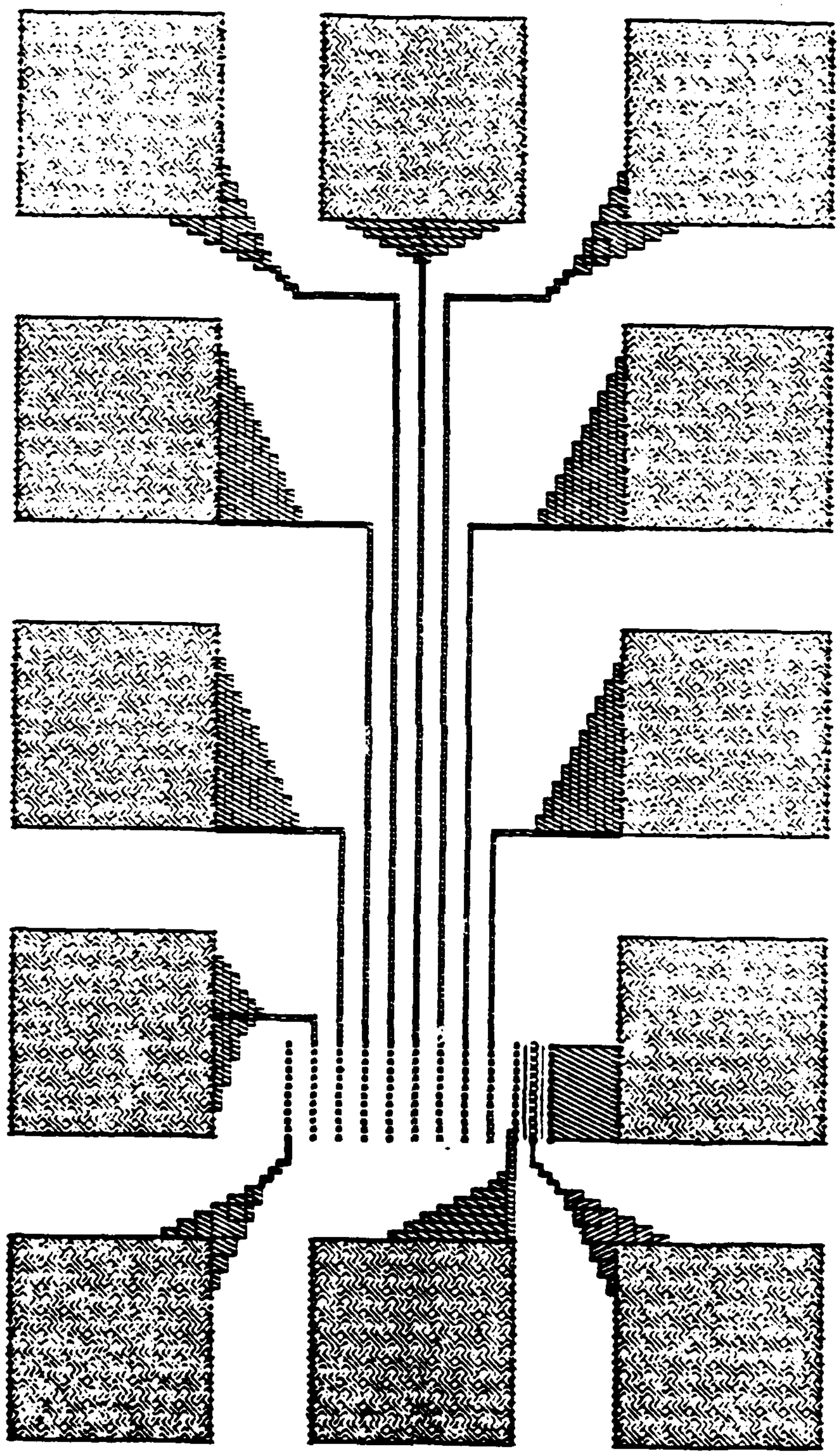


Fig. 4.2.2-1 Horizontal MESFET backgating test structure.

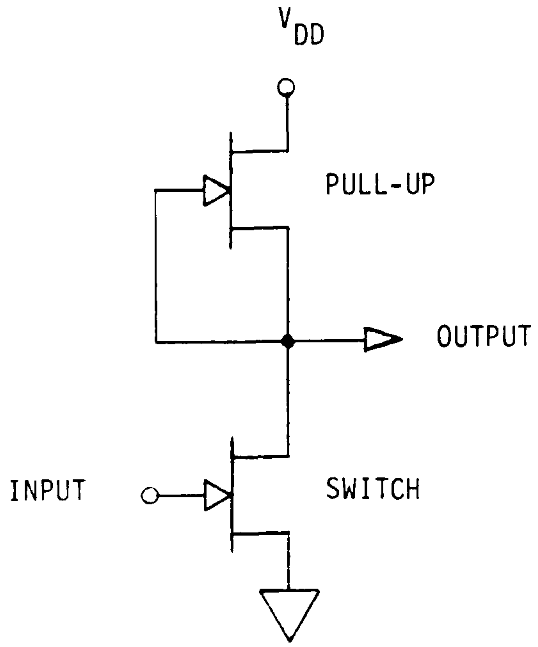


Fig. 4.2.2-2 Basic GaAs digital inverter.

Figure 4.2.2-3 shows the transistor connections and input waveforms for testing the pull-up device, and Fig. 4.2.2-4 shows the same information for the switching device.

Tests were made on devices selected from wafer lot No. 1, wafers 11 and 14. Data on wafer 11 (Figs. 4.2.2-5 through 4.2.2-10) indicate the severity of backgating effects even with conductors removed by relatively large distances (27 μm). Wafer 14 was proton-implanted to reduce the effects of backgating, as indicated in the results shown in Figs. 4.2.2-11 through 4.2.2-15.

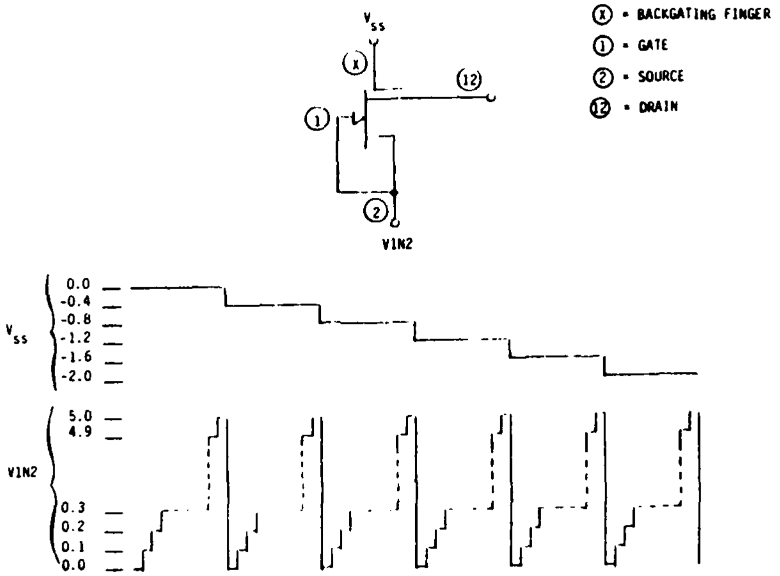


Fig. 4.2.2-3 Test setup for measuring backgating effect on horizontal transistor connected as a pull-up device.

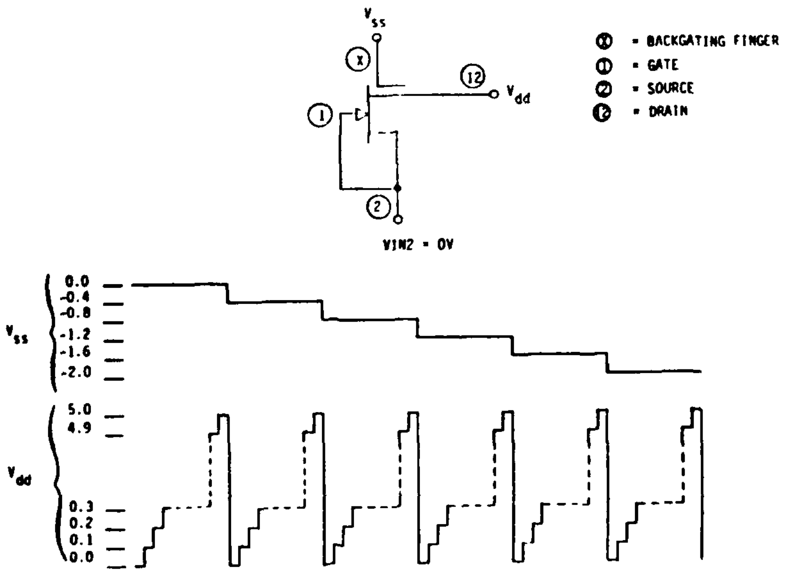


Fig. 4.2.2-4 Test setup for measuring backgating effect on horizontal transistor connected as a switch.

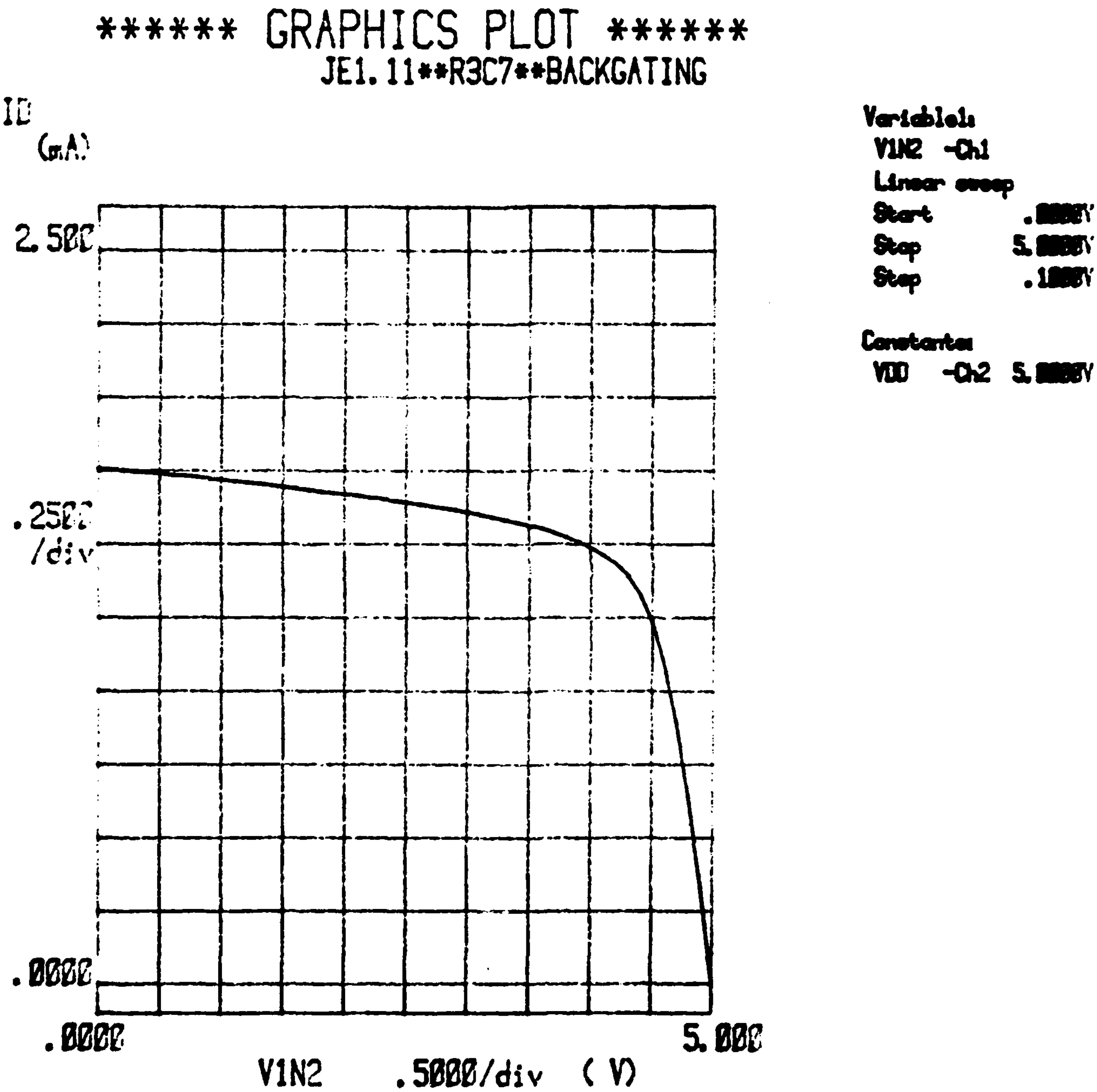


Fig. 4.2.2-5 Basic pull-up transfer curve without backgating.

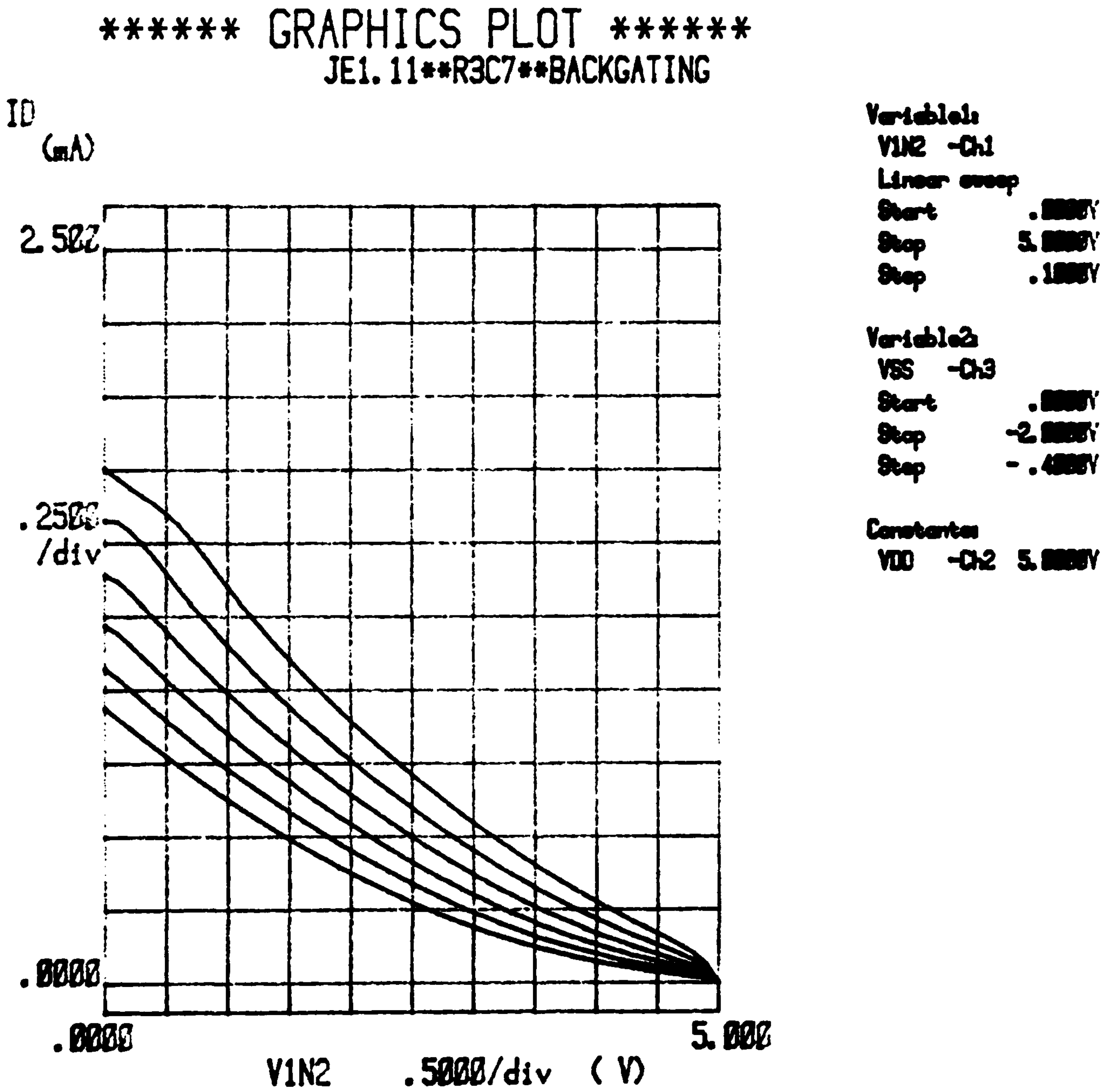


Fig. 4.2.2-6 Basic pull-up transfer curves with biased backgating finger 3 μm from drain.

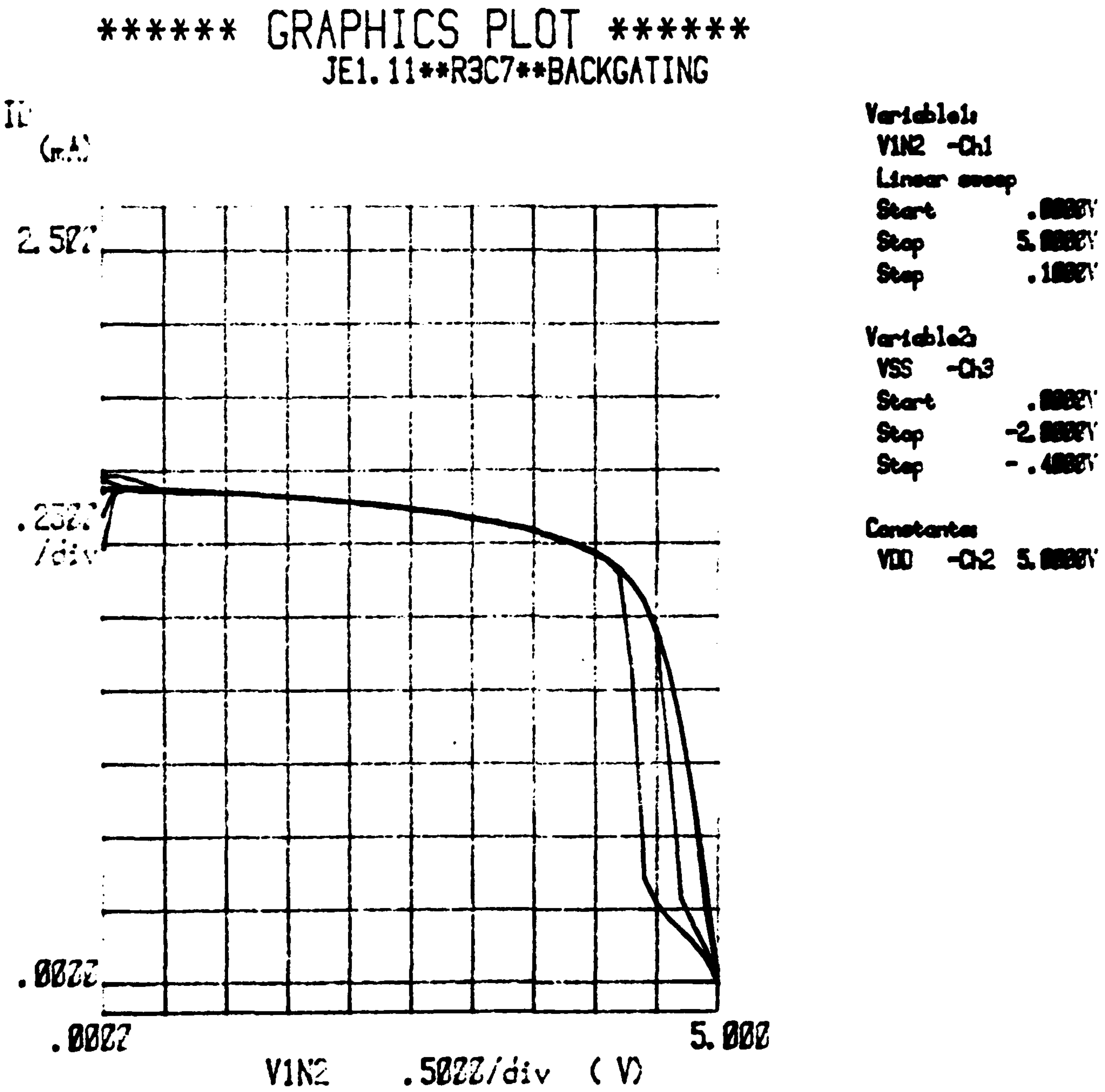


Fig. 4.2.2-7 Basic pull-up transfer curves with biased backgating finger 27 μm from drain.

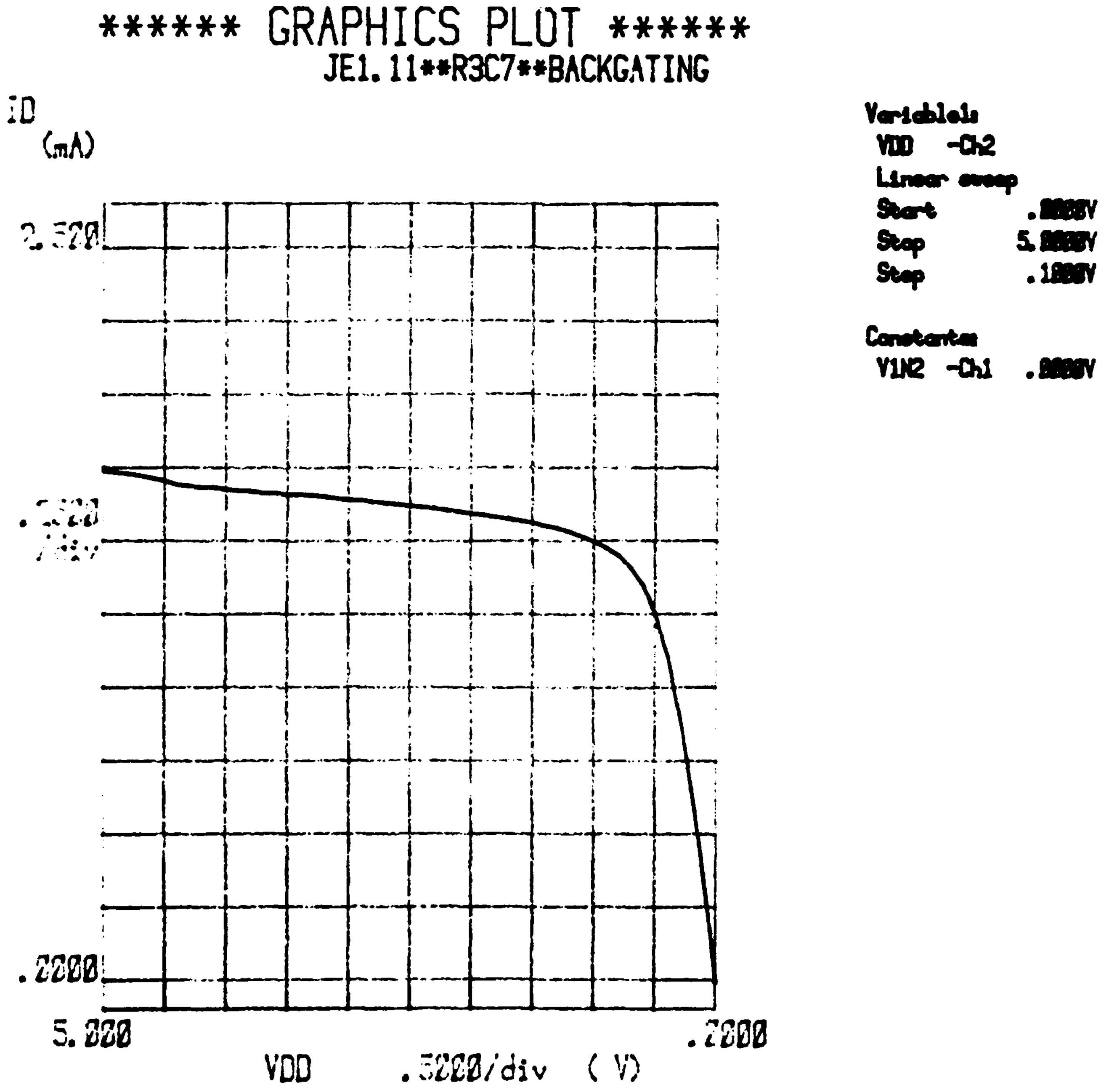


Fig. 4.2.2-8 Switch transfer curve without backgating.

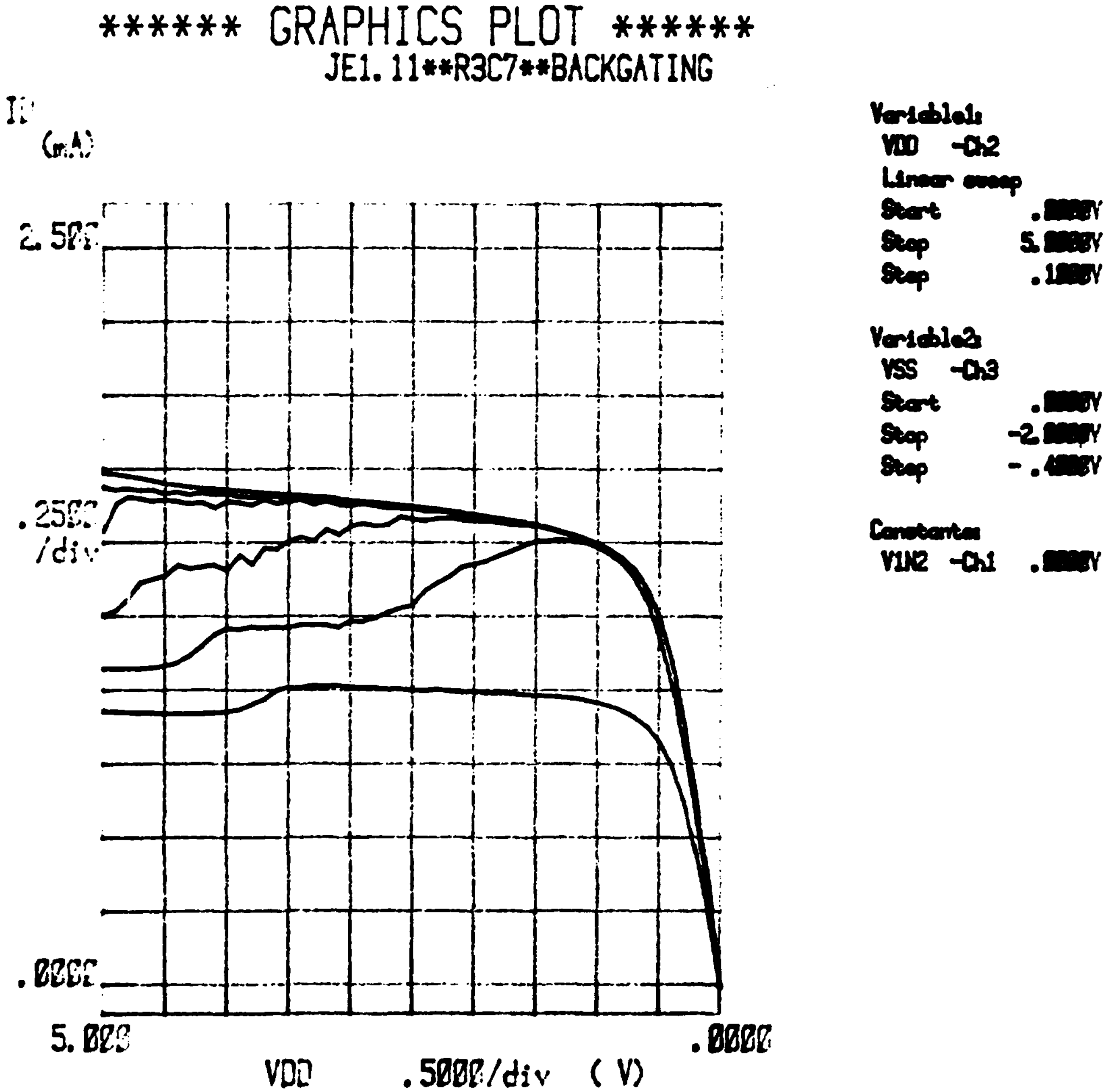


Fig. 4.2.2-9 Basic switch transfer curves with biased backgating finger 3 µm from drain.

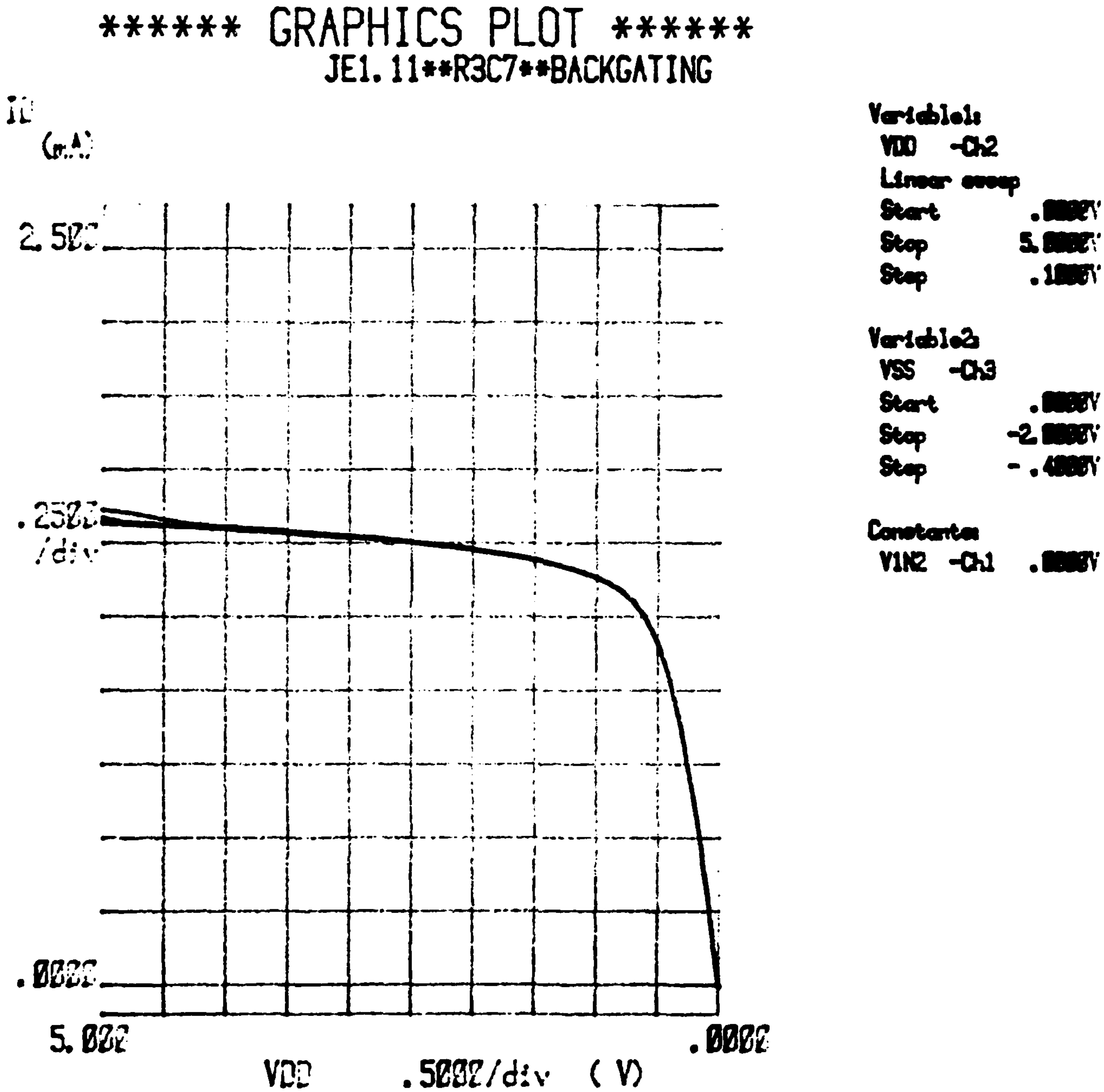


Fig. 4.2.2-10 Basic pull-up transfer curves with biased backgating finger 27 µm from drain.

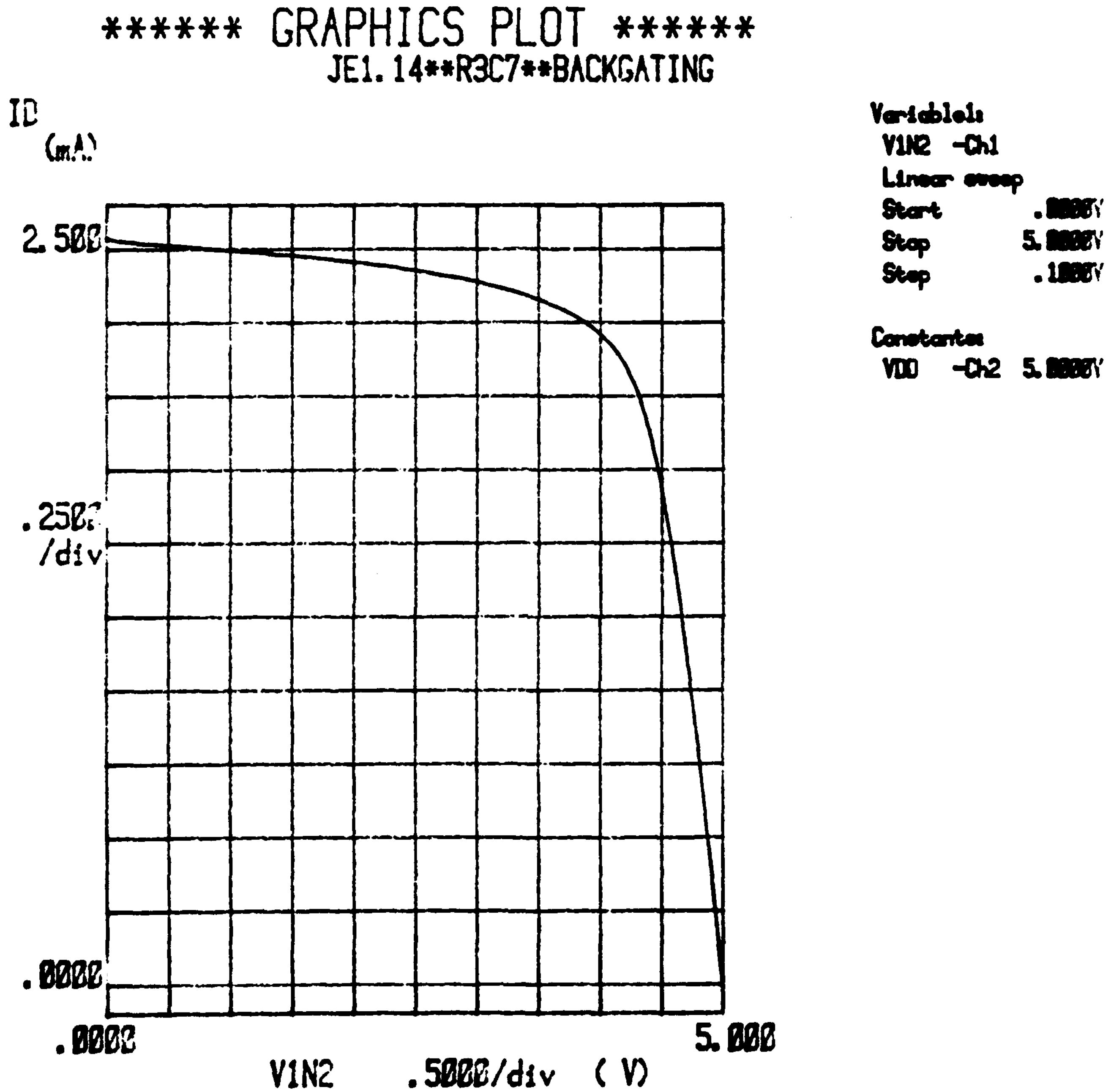


Fig. 4.2.2-11 Basic pull-up transfer curve without backgating.

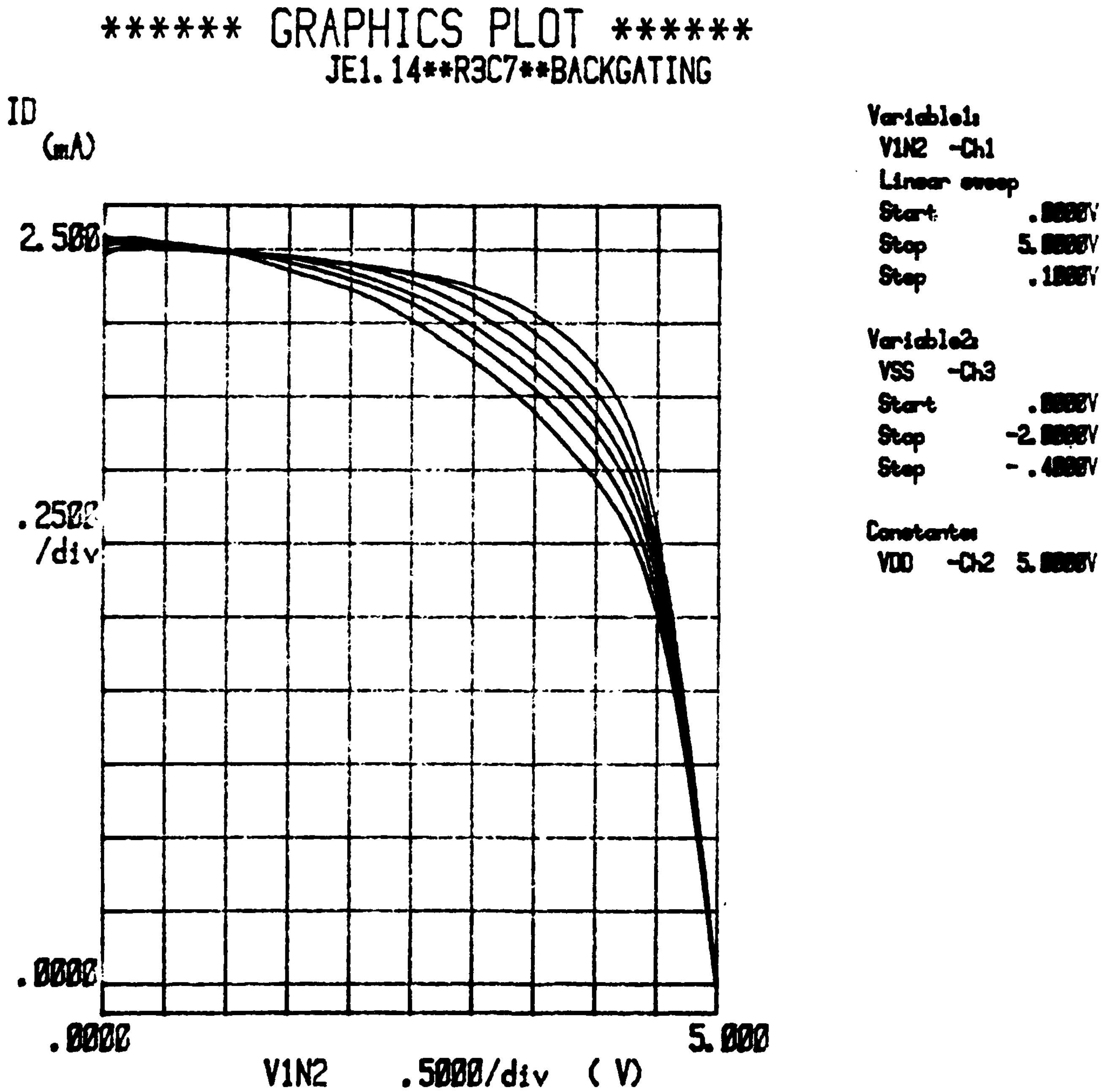


Fig. 4.2.2-12 Basic pull-up transfer curves with biased backgating finger 3 μm from drain.

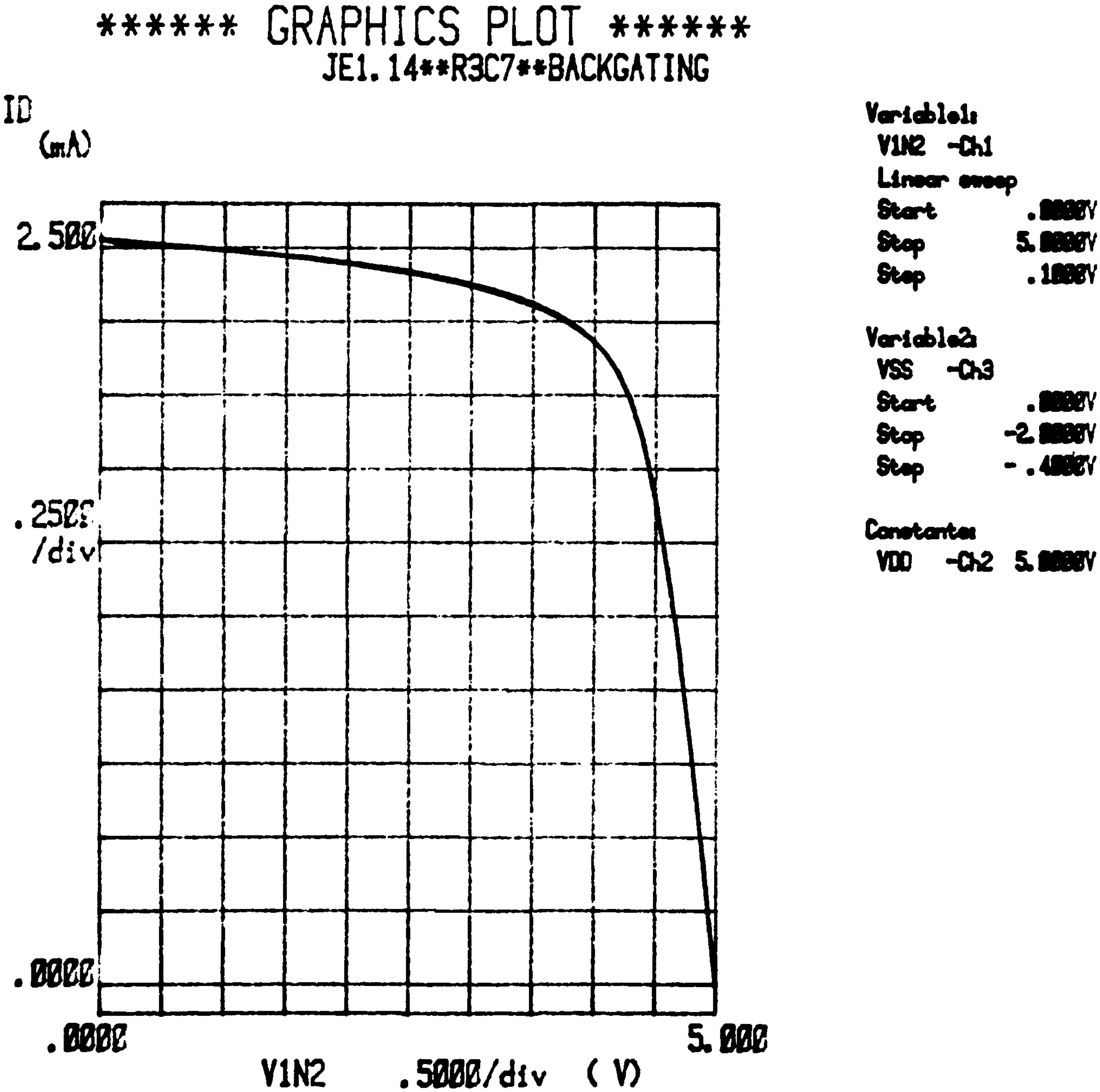


Fig. 4.2.2-13 Basic pull-up transfer curves with biased backgating finger 6 μm from drain.

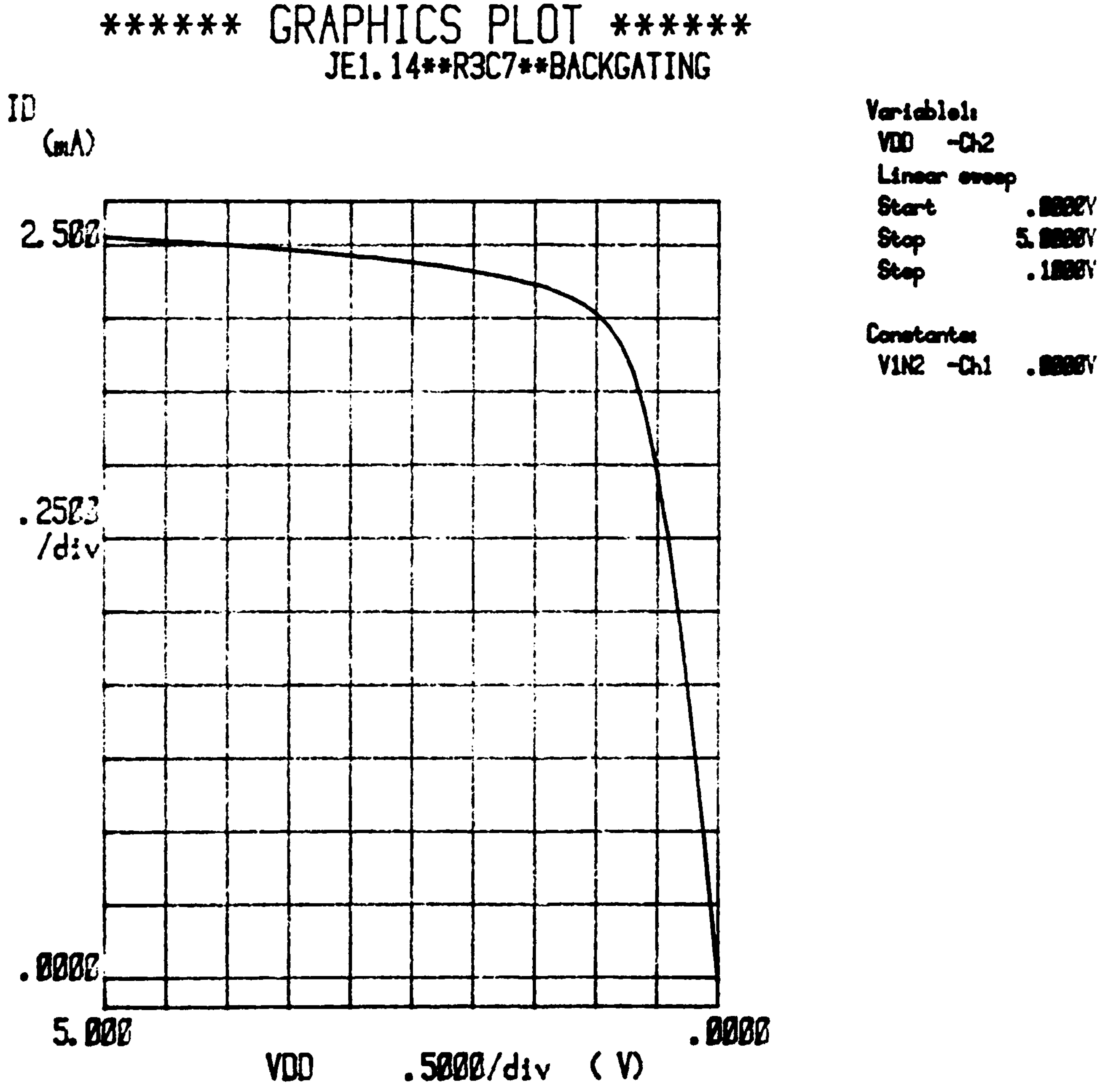


Fig. 4.2.2-14 Basic switch transfer curve without backgating.

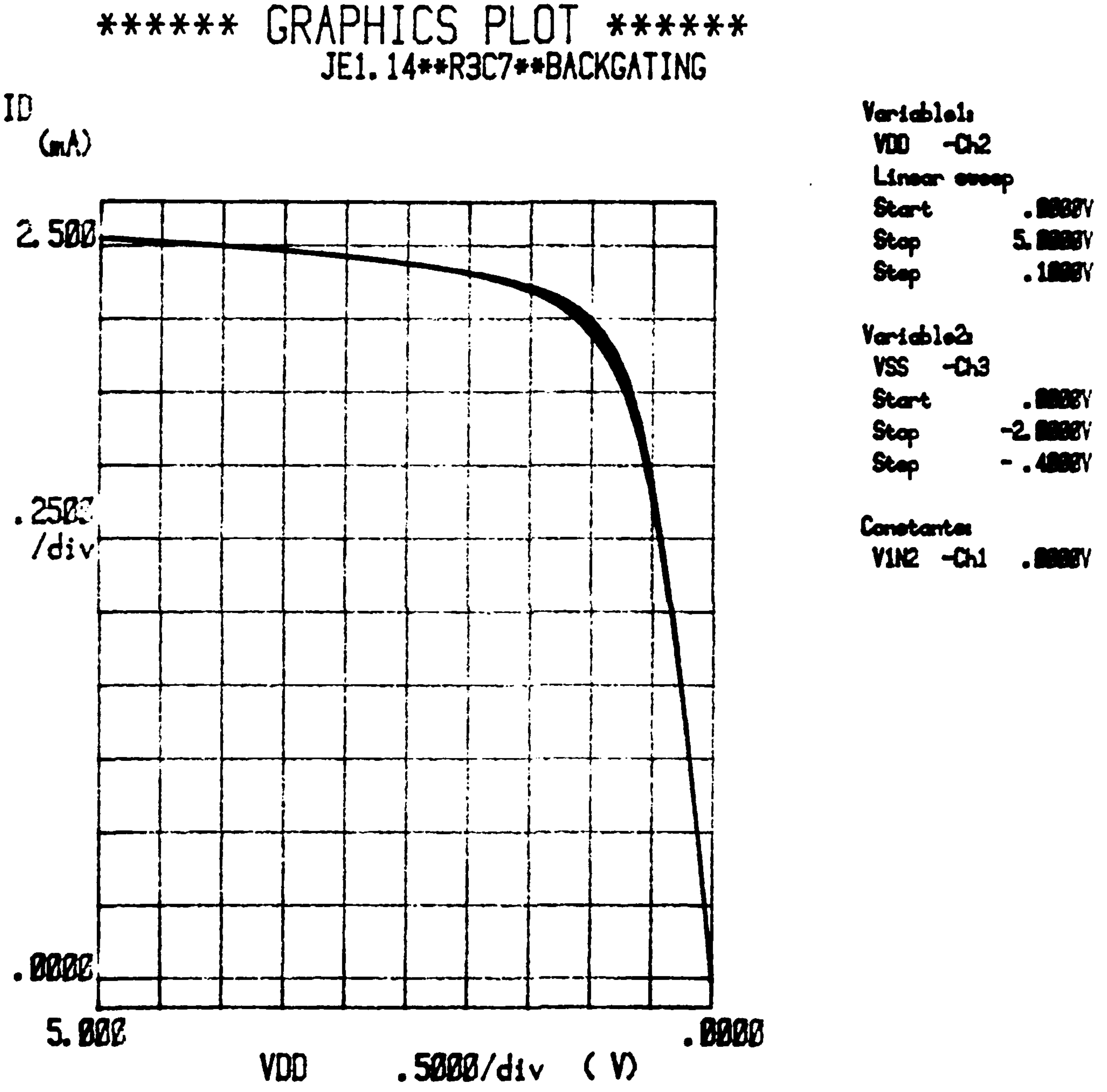


Fig. 4.2.2-15 Basic switch transfer curves with biased backgating finger 3 μm from drain.

4.2.3 Buffered FET Logic Parametric Test

Initial wafer probing concentrated on collecting dc parametric test data from the BFL test device No. 2 (BFLTD2) shown in Fig. 4.2.3-1. The tests performed are listed in Table 4.2.3-1, the test conditions are listed in Table 4.2.3-2, and an explanation of the test parameters is detailed in Table 4.2.3-3. Data was collected from two of five test sites (Fig. 4.2.3-2), within each of the 44 micro die locations on a wafer, and the average was plotted as shown in the following data (Figs. 4.2.3-3 through 4.2.3-11).

Details of the date from all nine tests have been previously reported in the Monthly Progress Report C82-763.11/501. To minimize repetitive reporting of data, results from tests 1, 6, 7 and 9 will be included in this report. The data indicate good parametric control.

4.2.4 Bidirectional Output Drivers

Three output drivers were designed (Sec. 2.4.5, this report) for this project, which were tested and reported on. The output driver used on all circuit designs is shown in Fig. 4.2.4-1. A photograph of the output waveform of an operational device is shown in Fig. 4.2.4-2. The upper trace is the waveform across a 50 Ω terminating resistor tied to ground, and the lower trace is the drive voltage to the final stage (source follower output). The power supply voltages were set at $V_{DD} = V_{BB} = +2.5$ V and $V_{SS} = -2.0$ V. The output voltage on this particular device indicates excellent drive characteristics for a logic "0" (0 to 0.5 V) and a logic "1" (+1.5 to +2.0 V). all output drivers are tied to a separate power bus, V_{BB}, which can be adjusted to meet various output driver requirements.

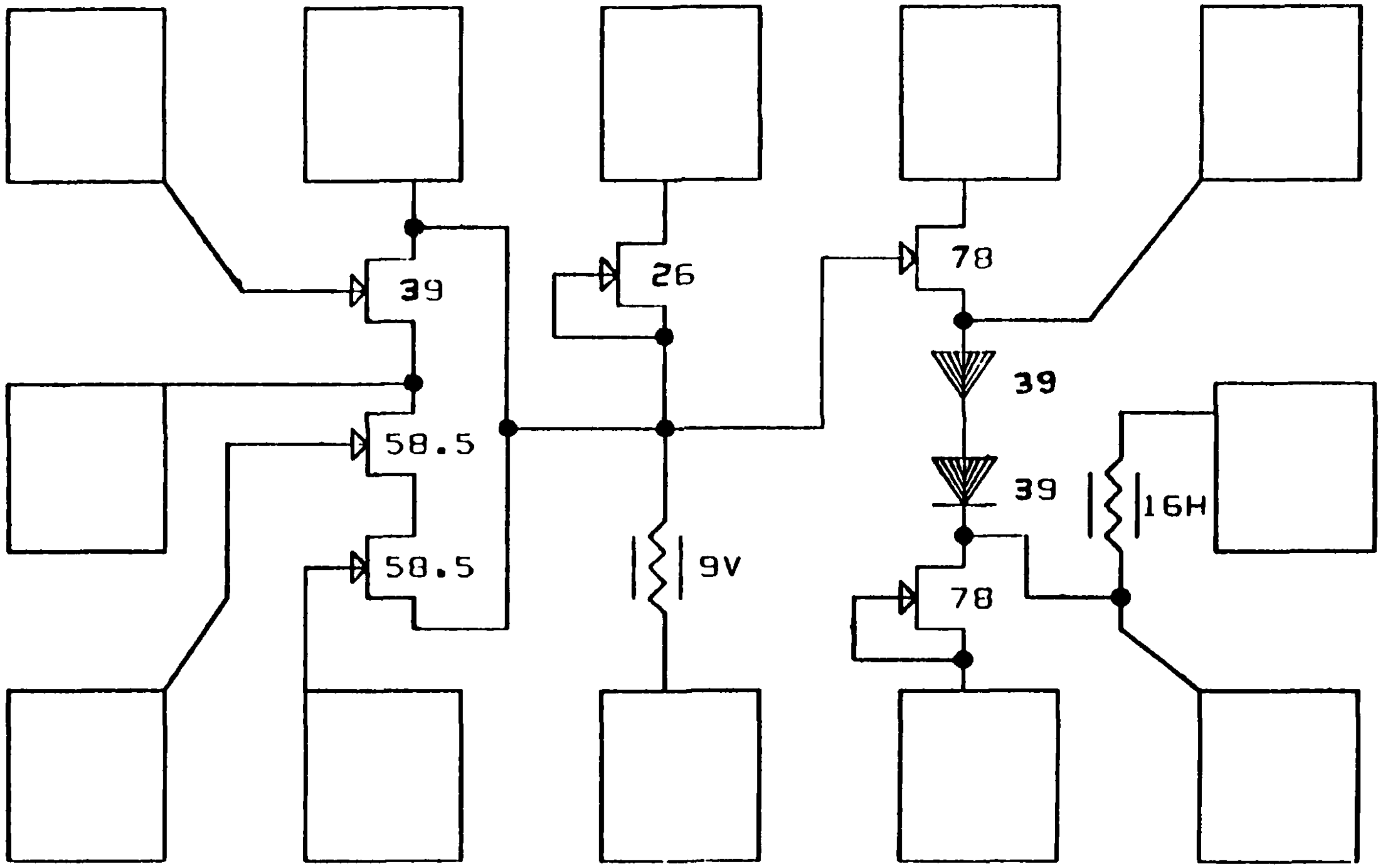


Fig. 4.2.3-1 Buffered FET logic test device 2 (BFLTD2).

Table 4.2.3-1

BFLTD2 Parametric Test

Test No.	Parametrics Measured
1	I/V characteristics of a 39 μm wide MESFET
2	I/V characteristics of two 58.5 μm wide series-connected MESFETs
3	I/V characteristics of a 26 μm wide pull-up MESFET
	I/V characteristics of a 9 μm wide vertical saturated resistor
4	I/V characteristics of a 78 μm wide pull-down MESFET
	I/V characteristics of a 16 μm wide horizontal saturated resistor
5	I/V characteristics of a 78 μm wide source follower MESFET
6	I/V characteristics of two 39 μm x 2 μm series diodes
7	Transfer curve characteristics of a MESFET inverter
8	Transfer curve characteristics of a MESFET/saturated resistor inverter
9	Transfer curve characteristics of a MESFET/diode source follower

Table 4.2.3-2

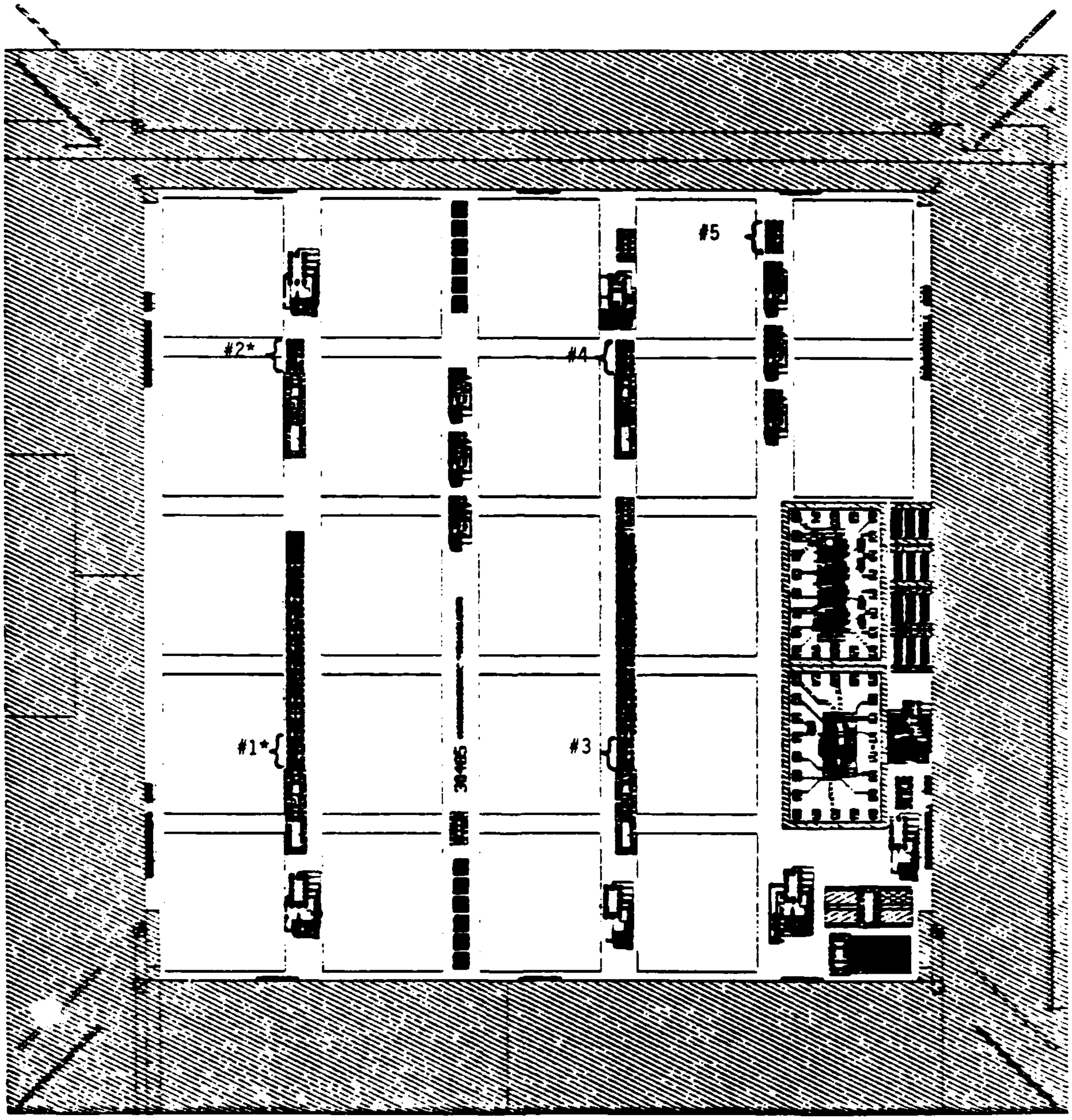
Test Conditions

Test No.	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
	BFLTD2 Pad Numbers											
1	V2	V1	V1								V4/I1	V3
2	V2	V3	V3								V4/I2	Va
3				V3/I4						V3/I3	V2	
3					V5/I6	V2	V5/I5					
5								V2	V5/I7		V6	
6								V2		V7/I8		
7	V2	V8	V8		V1	V01			V10	V10		V9
8	V2	V8	V8	V10		V02	V1		V10			V9
9					V11	V03			V10		V12	

Table 4.2.3-3

Test Parameter Definition

Input and Bias Voltages	Output Measurements	
V1 = -2.0 V	I1 -	
V2 = Ground	I2 -	
V3 = -1.2 to +0.8 V (sweep)	I3 -	
V4 = 0.0 to +4.0 V (1 V steps)	I4 -	Current
V5 = 0.0 to +4.0 V (sweep)	I5 -	
V6 = +0.8 to -1.2 V (sweep)	I6 -	
V7 = +2.0 to -18.0 V (sweep)	I7 -	
V8 = -1.1 V	I8 -	
V9 = -1.4 to +0.6 V (sweep)	V01 -	
V10 = +2.5 V	V01 -	Voltage
V11 = -2.0 V; -1.0V	V03 -	
V12 = -0.0 to +2.5 V (sweep)		



*Selected Test Sites

Fig. 4.2.3-2 Buffered FET logic (BFL) test sites.

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1
TEST # 1 - P4 VOLTAGE VS I4 CURRENT (UA)
DIE AVERAGE FROM 38 DIE

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

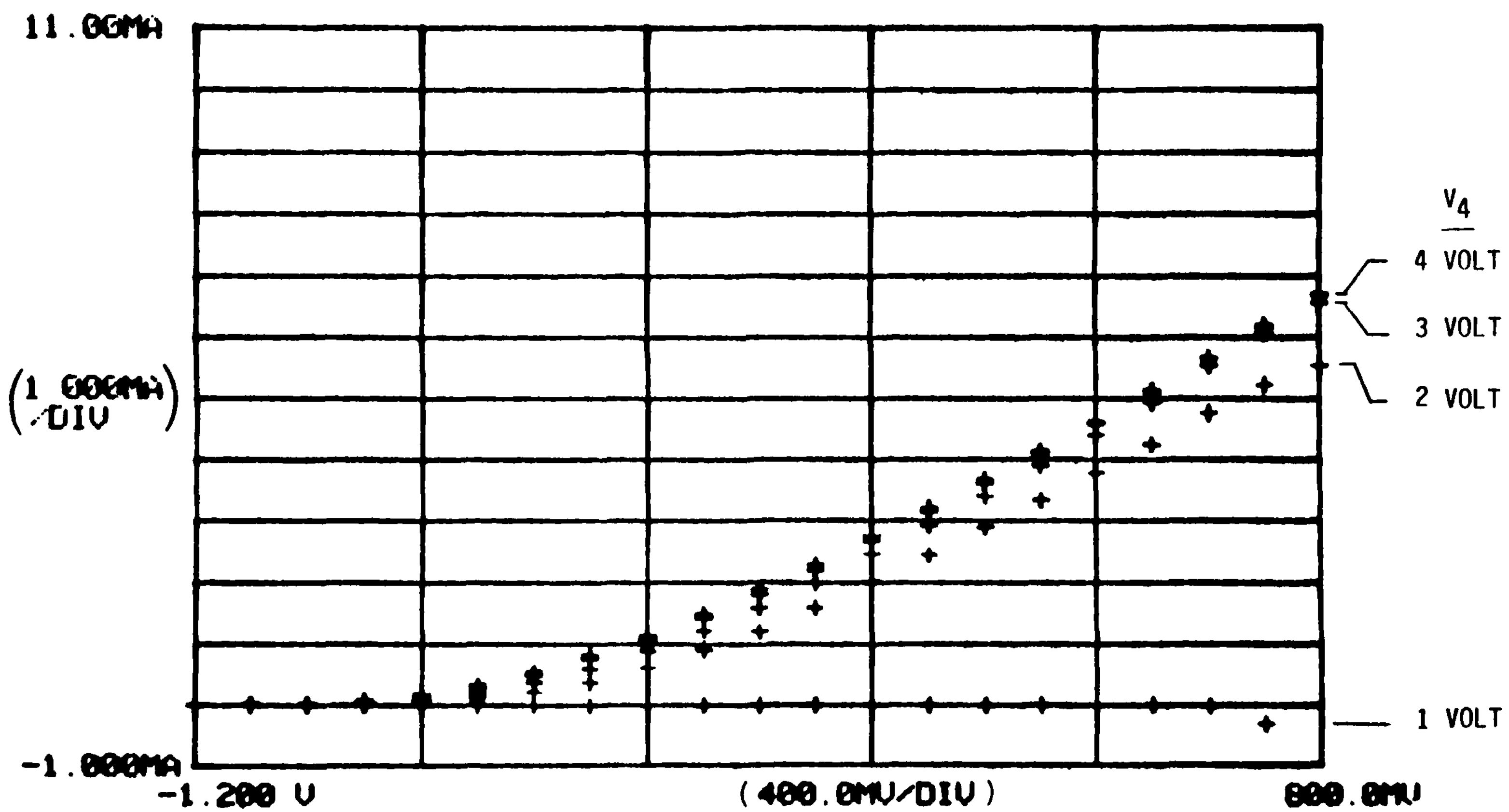


Fig. 4.2.3-3 Test number 1 results.

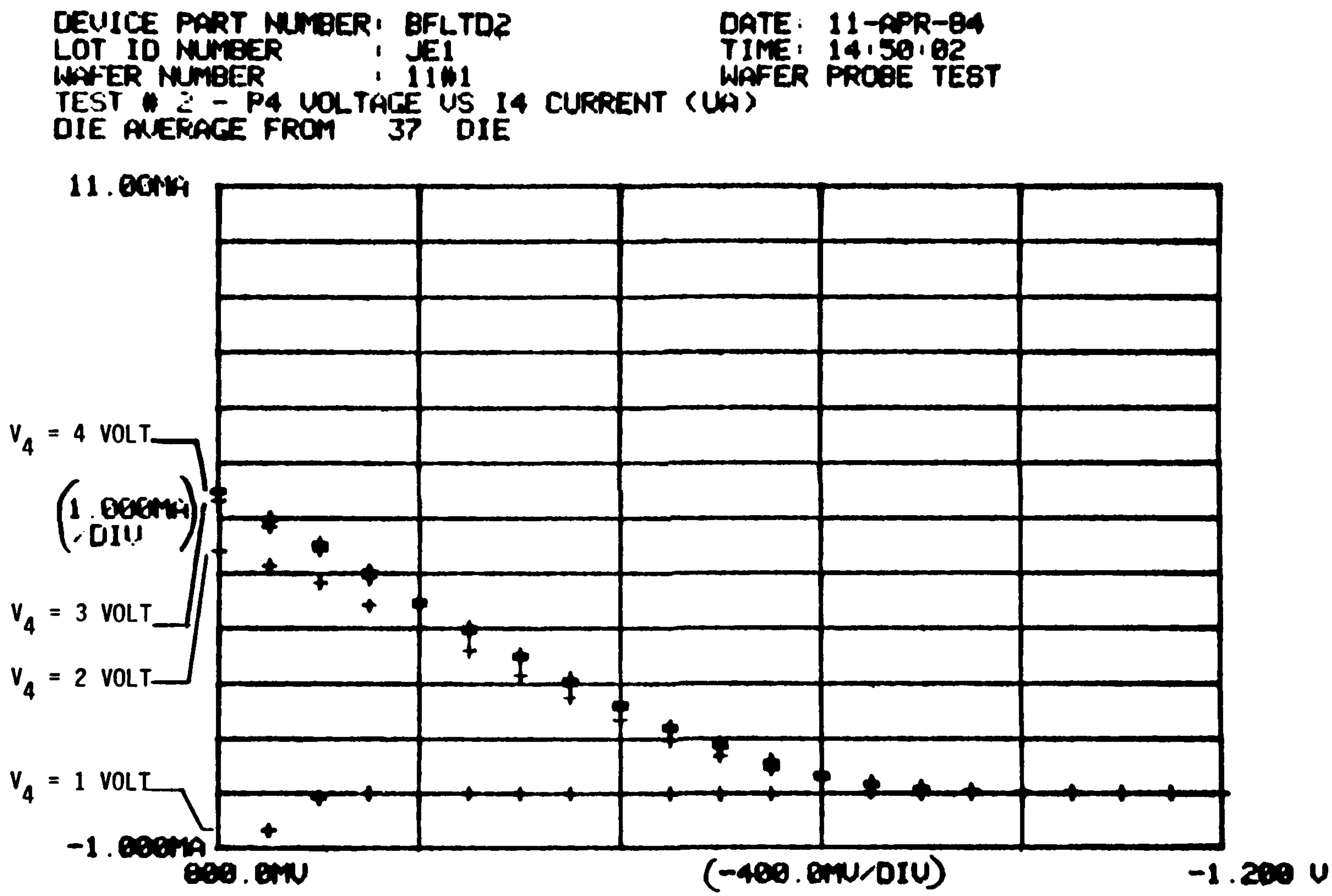


Fig. 4.2.3-4 Test number 2 results.

DEVICE PART NUMBER: BFLTD2 DATE: 18-APR-84
LOT ID NUMBER : JE1 TIME: 15:25:29
WAFER NUMBER : 11#2 WAFER PROBE TEST
TEST # 3 - P5,P11 VOLTAGE VS P5,P11 CURRENT (UA)
DIE AVERAGE FROM 22 DIE

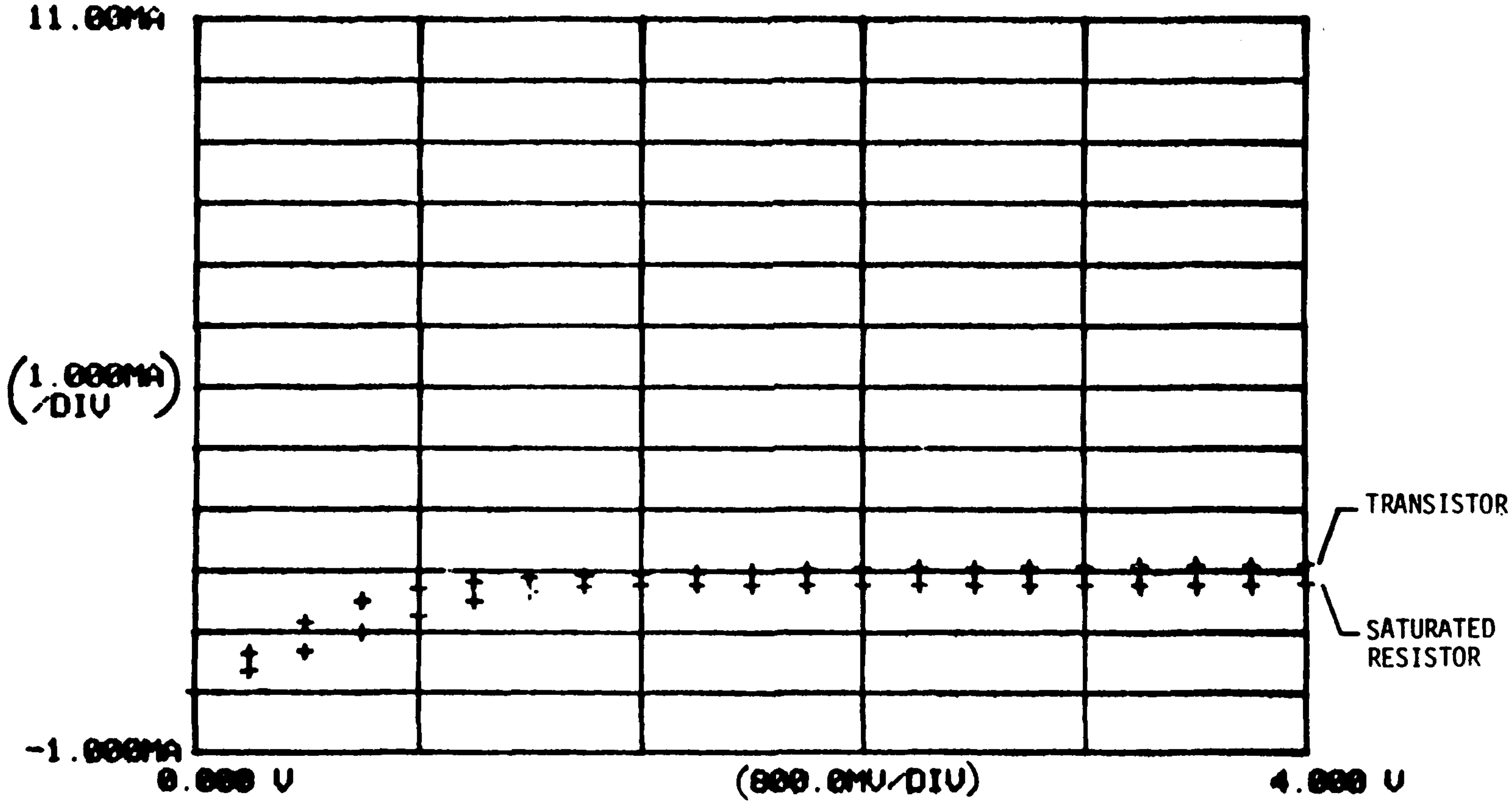


Fig. 4.2.3-5 Test number 3 results.

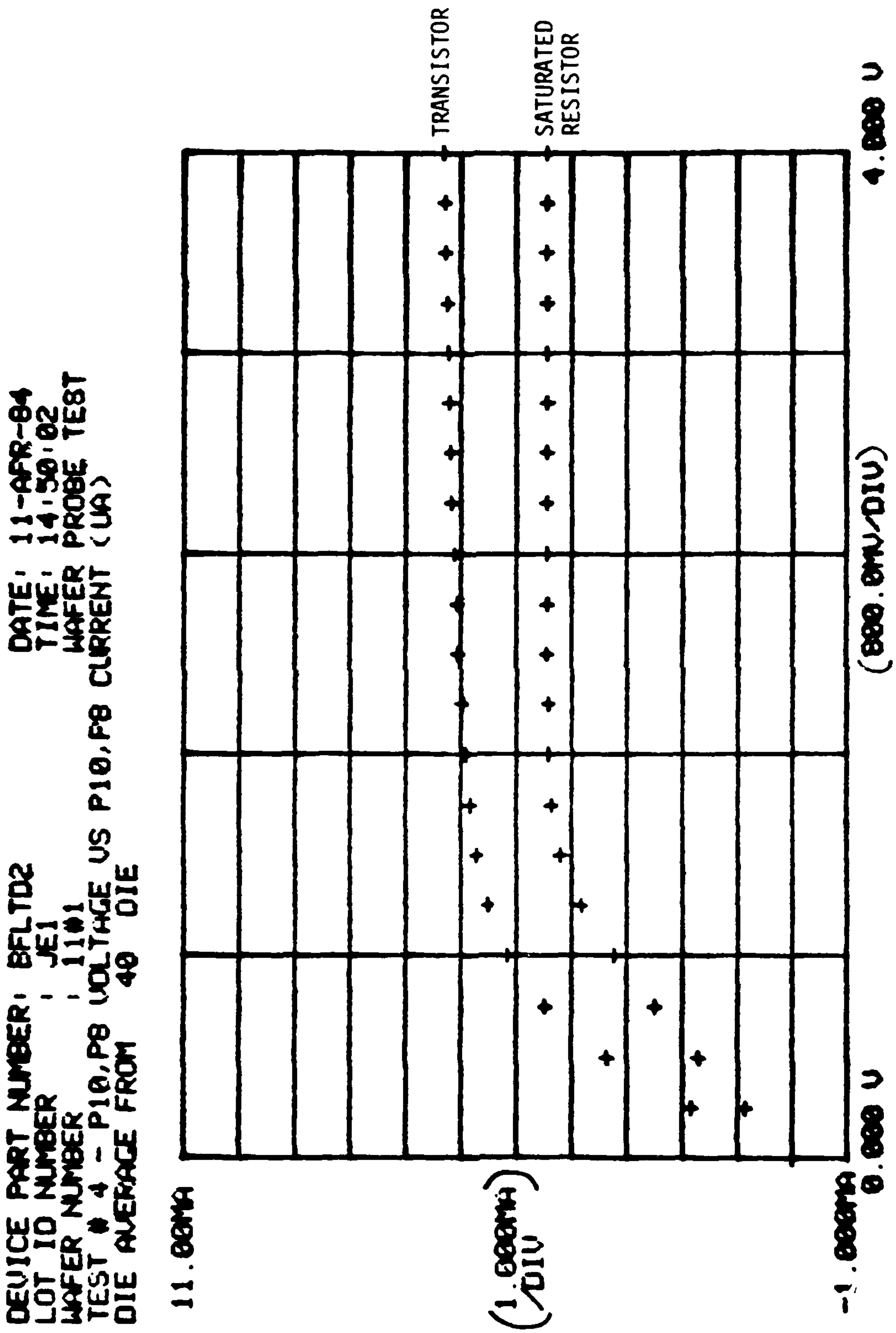


Fig. 4.2.3-6 Test number 4 results.

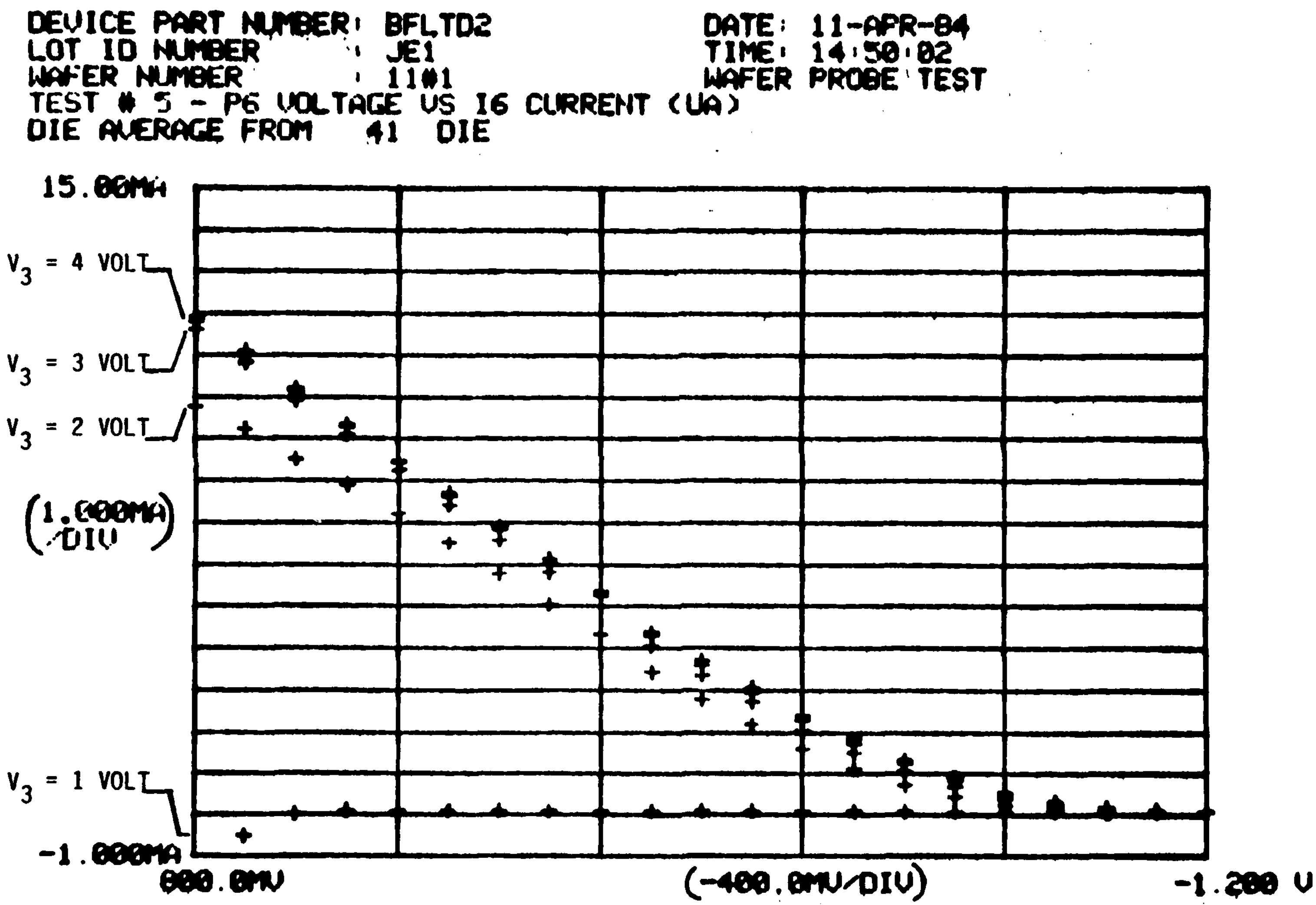


Fig. 4.2.3-7 Test number 5 results.

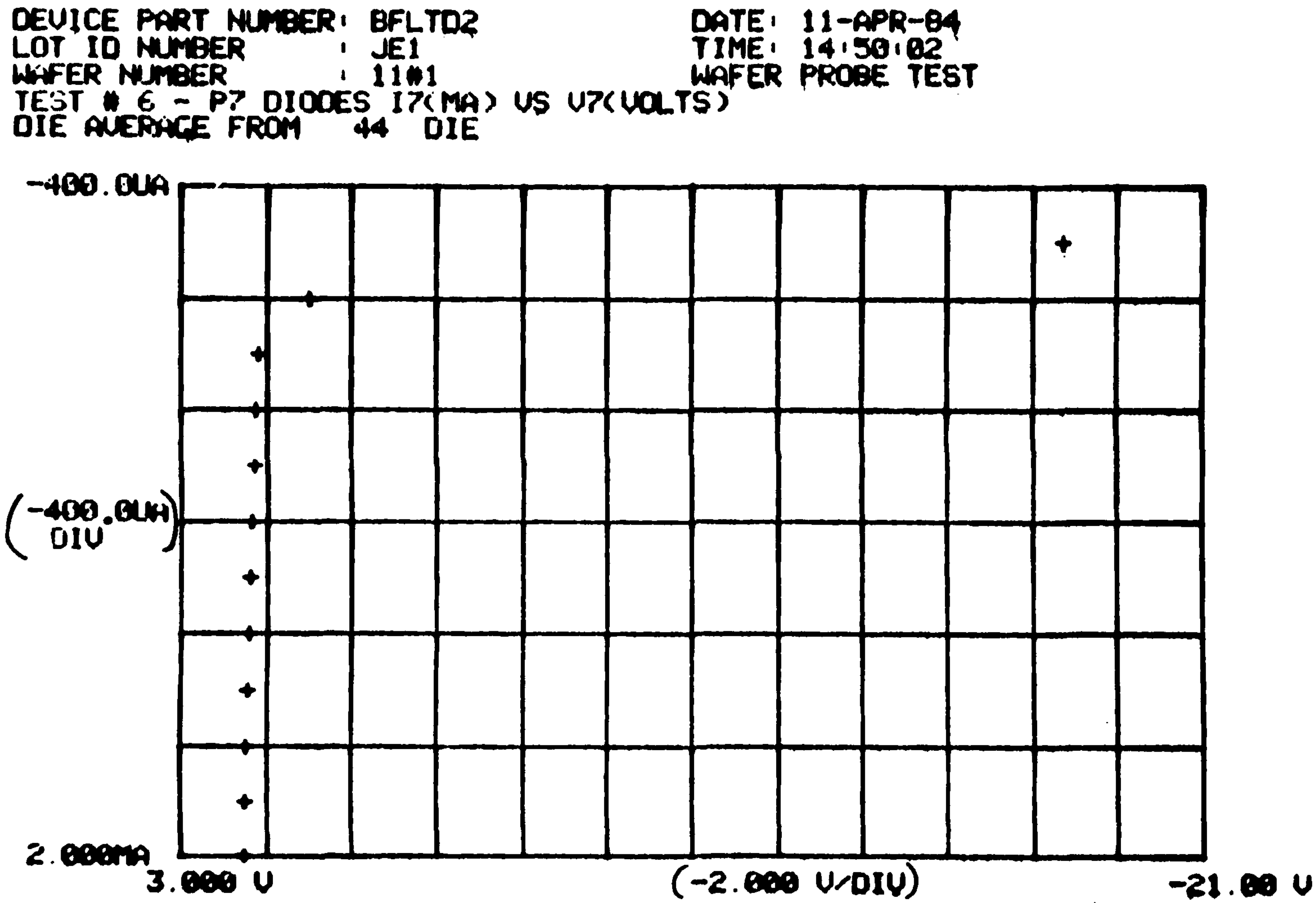


Fig. 4.2.3-8 Test number 6 results.

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#2

DATE: 18-APR-84
TIME: 15:25:29
WAFER PROBE TEST

TEST # 7 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - FET RESISTORS
DIE AVERAGE FROM 38 DIE

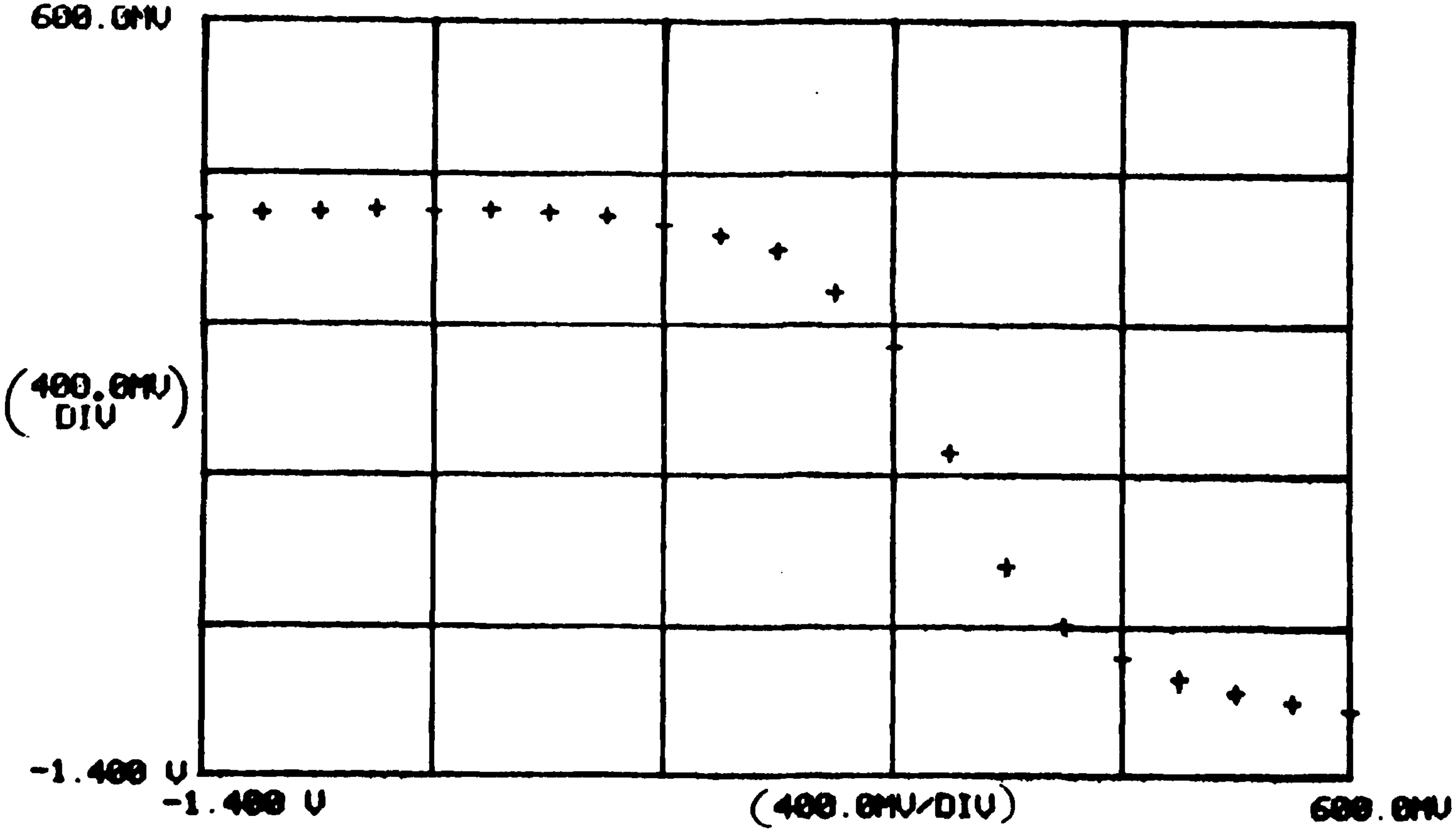


Fig. 4.2.3-9 Test number 7 results.

DEVICE PART NUMBER: BFLTD2
LOT ID NUMBER : JE1
WAFER NUMBER : 11#1

DATE: 11-APR-84
TIME: 14:50:02
WAFER PROBE TEST

TEST # 8 - P3 INPUT VOLTAGE VS P9 OUTPUT VOLTAGE - SAT RESISTORS
DIE AVERAGE FROM 40 DIE

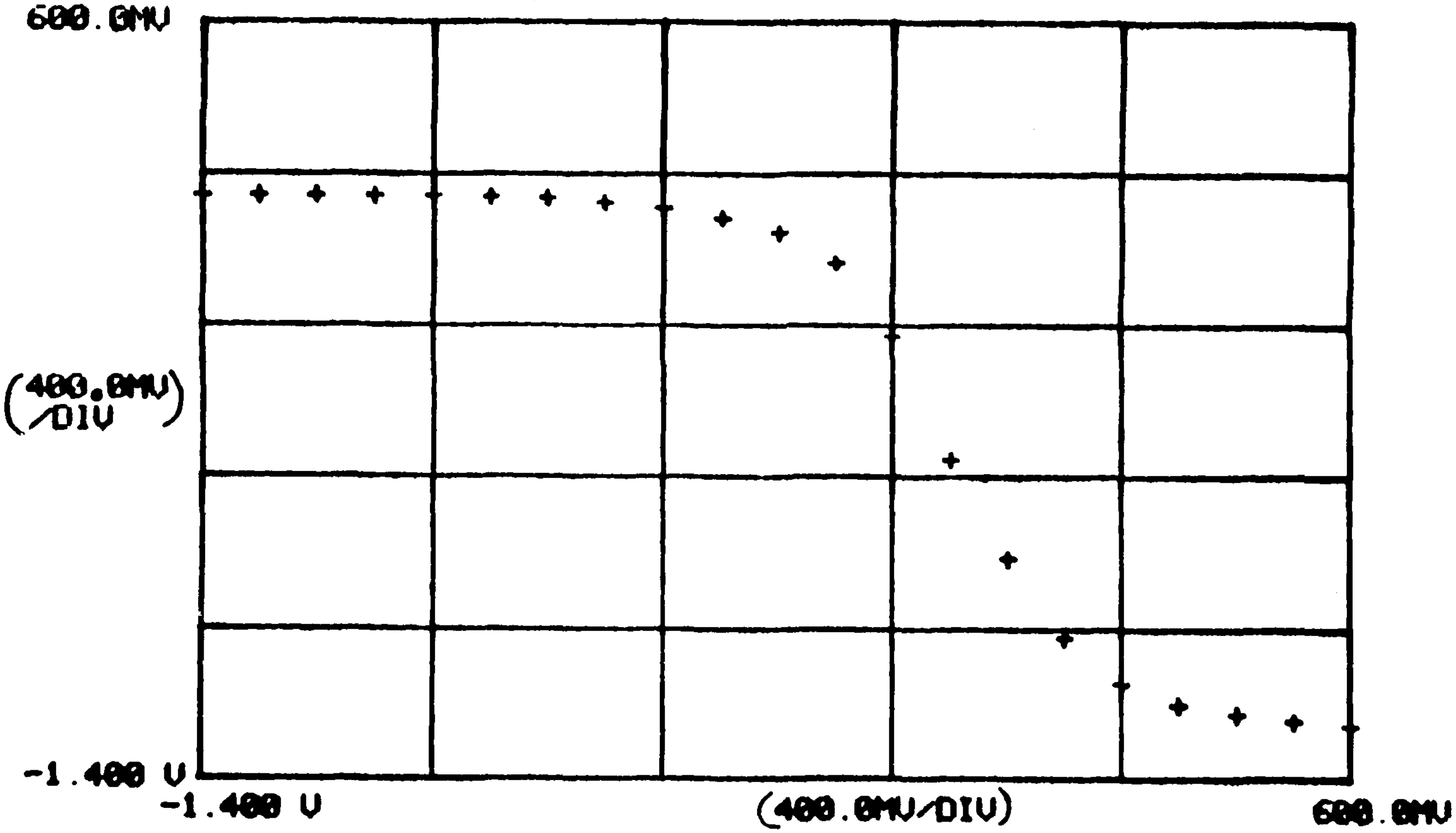


Fig. 4.2.3-10 Test number 8 results.

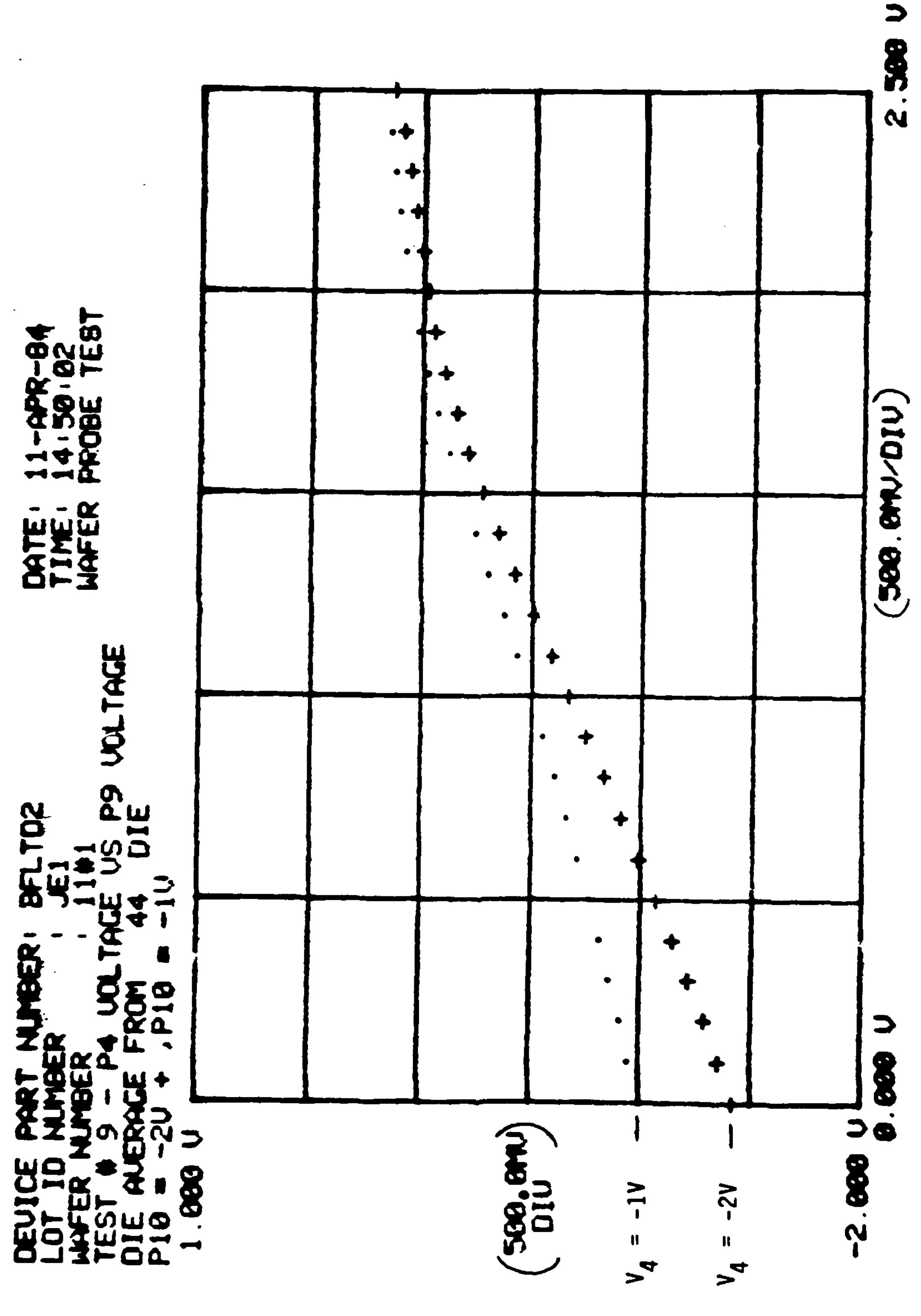


Fig. 4.2.3-11 Test number 9 results.

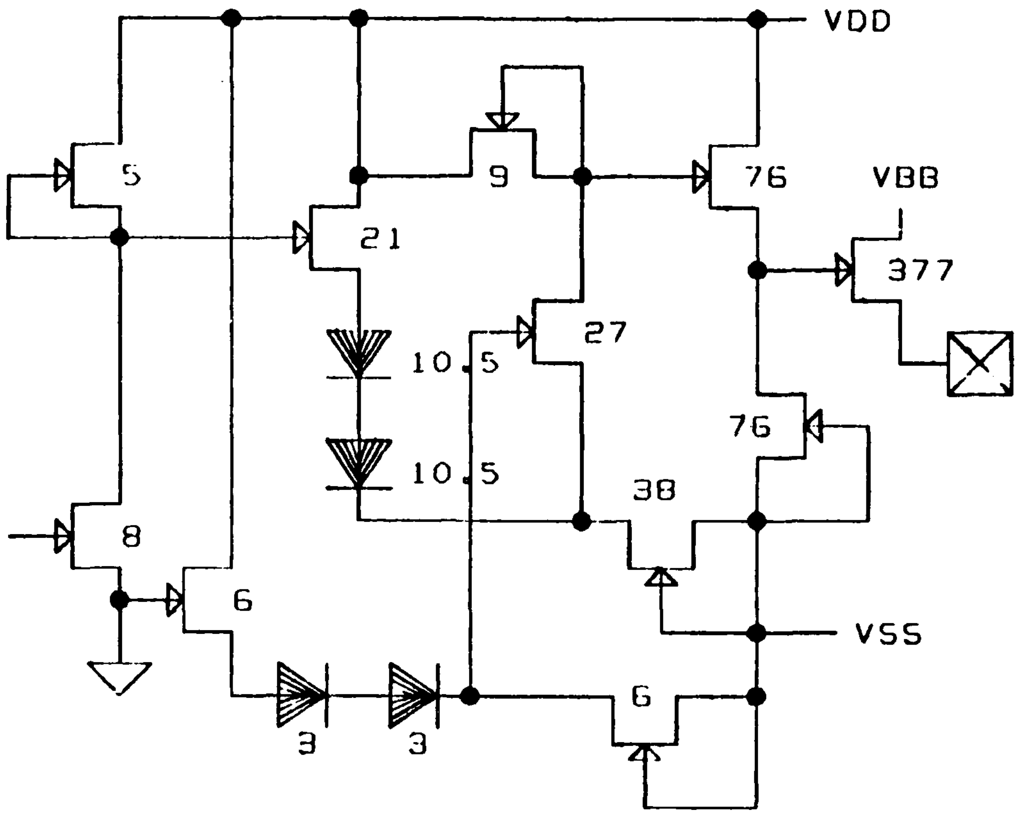


Fig. 4.2.4-1 Bidirectional output driver for driving 50 Ω lines (all FETs).

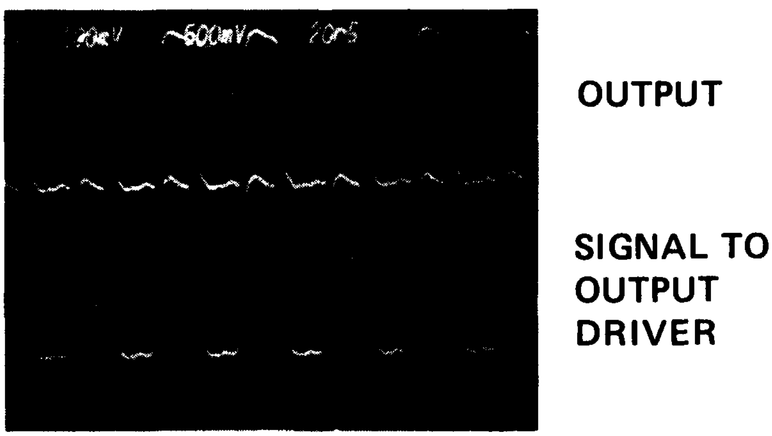


Fig. 4.2.4-2 All FET driver waveforms.

4.2.5 Memory Latches

A circuit diagram of the memory latch device included in the test structures is shown in Fig. 4.2.5-1. Tests were performed to determine operability of the device. However, a design error precluded the collection of any test data. The feedback networks within the device made it impossible to microprobe to locate the fault.

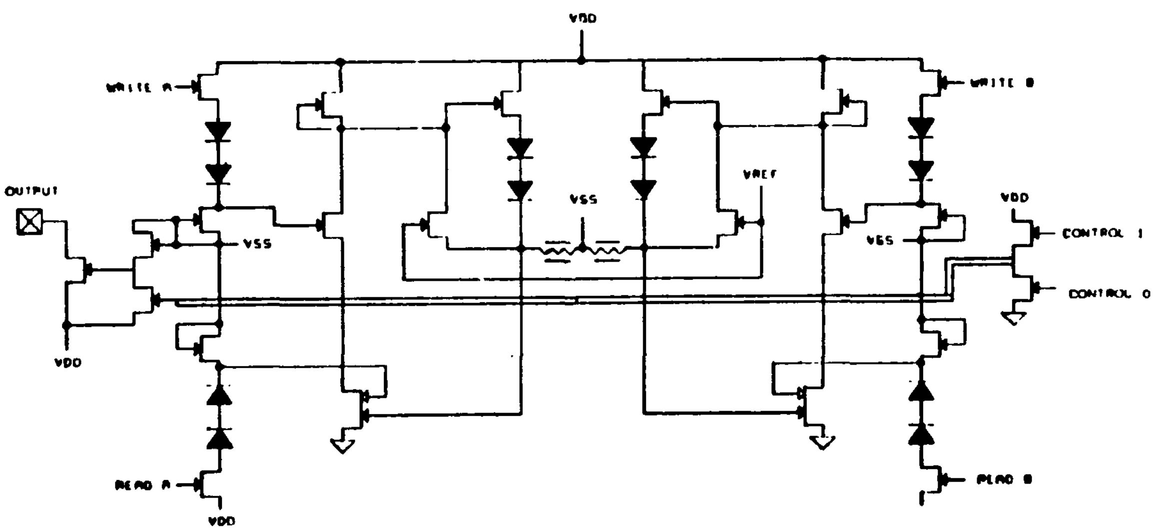


Fig. 4.2.5-1 Memory latch.

5.0 YIELD, PACKAGING AND DELIVERY DATA

Three wafer lots, of four wafers each, were processed for this project and include the following:

Lot 1: JE1-11, 12, 13, 14
Lot 2: JE1-21, 22, 23, 24
Lot 3: JE1-31, 32, 33, 34

Lot 2 was scrapped due to photoresist adhesion problems during the Schottky metalization step, which caused metal bridging within the circuit elements. Lot 3 was a backup to Lot 1, which was used to collect test data. Two wafers from Lot 1, JE1-11 and JE-114, were mainly tested and the results compared, since the latter wafer was proton-implanted, while wafer JE1-11 was not.

5.1 Wafer Probe Yield Data

Wafer probe yield data on basic circuit elements are listed in Table 5.1-1. As indicated, the yield was greatest for the circuits which were not proton-implanted. With the limited data available, we do not know if this is an effect of the implant or just differences between the wafers.

There are 44 major die locations of fixed dimensions on each wafer. To accommodate the fixed die size, multiple circuit cells are placed within the given area, as shown in Fig. 5.1-1. To make use of the available space, certain cells were repeated, based on mutual agreement between ERADCOM and Rockwell International.

Figures 5.1-2 and 5.1-3 show a wafer map of the functional devices as listed in Table 5.1-1.

Table 5.1-1
Wafer Probe Yield

Part No.	Function	Wafer JE1-14 Yield Count	Wafer JE1-14 Yield (%)	Wafer JE1-11 Yield Count	Wafer JE1-11 Yield (%)
D30457	4-bit up/down counter	123 of 220	56	161 of 220	73
D30458	÷ 6/7, 10/11, 20/21, 40/41 prescalers	31 of 88	35	61 of 88	69
D30459	4-bit accumulator	66 of 176	37	131 of 176	74
D30462	Phase detectors	99 of 176	56	104 of 176	59
D30463	4-bit shift register	52 of 88	59	56 of 88	63
Totals		371 of 748	49	513 of 748	69

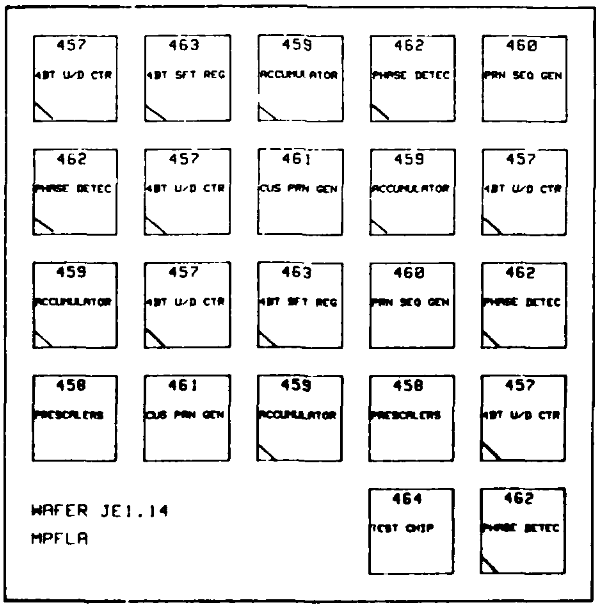


Fig. 5.1-1 Placement of circuit elements within each major die location.

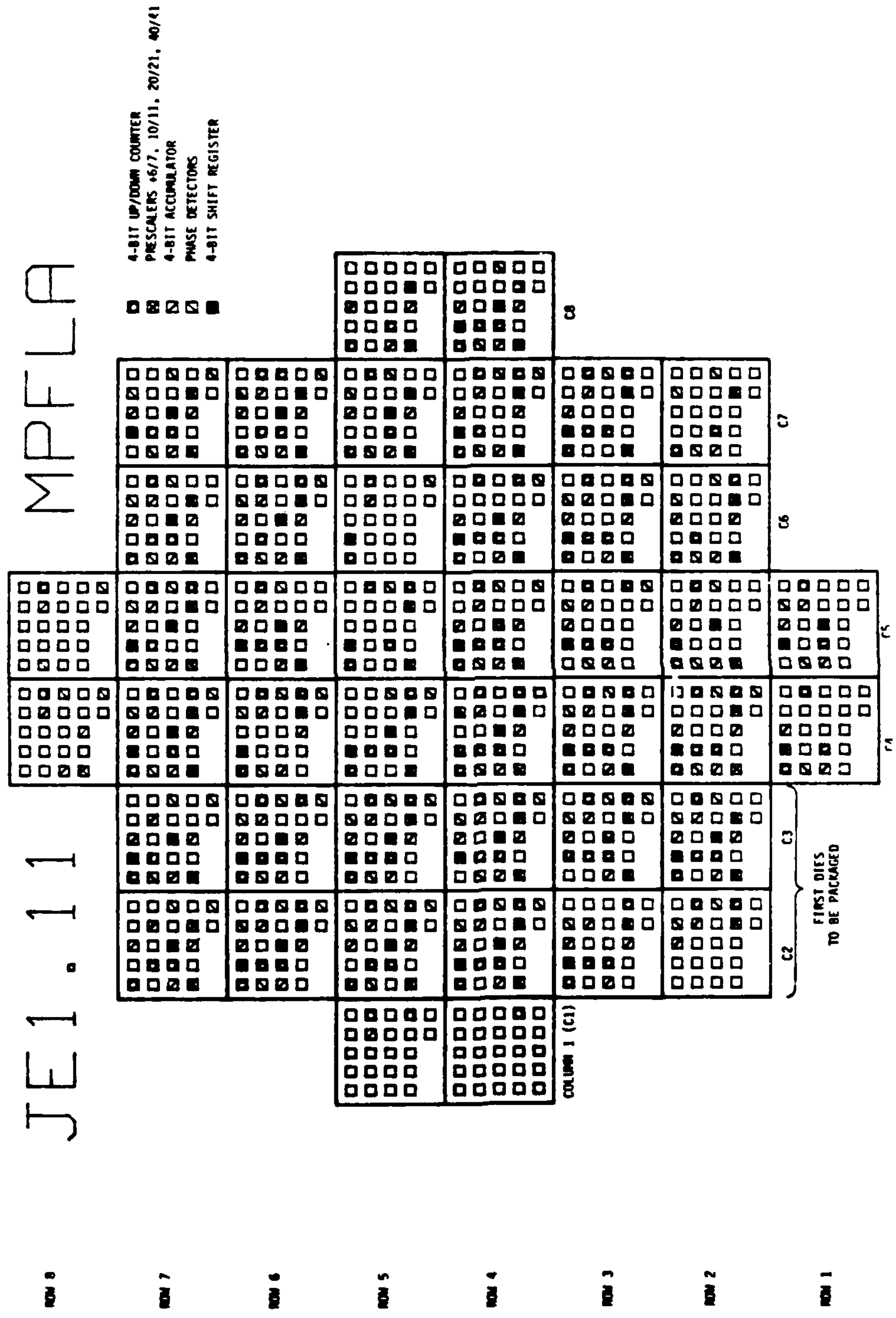


Fig. 5.1-2 Wafer map indicating fully functional devices to be packaged.

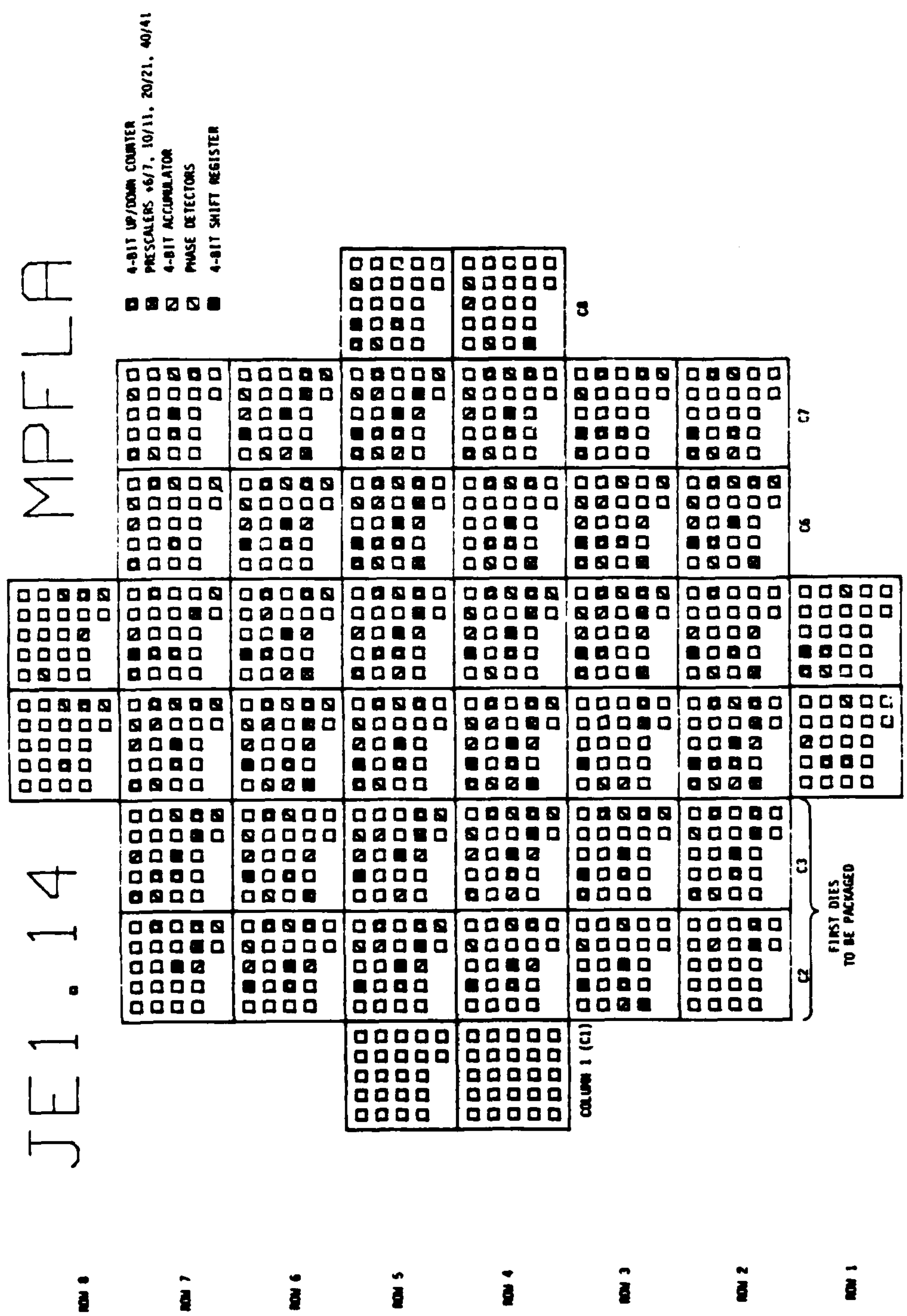


Fig. 5.1-3 Wafer map indicating fully functional devices to be packaged.

5.2 Packaged Parts

To perform the full speed test, as reported in Sec. 4.1, a large number of parts (265) were packaged, as indicated in Table 5.2-1; however, only a small portion of these devices were tested due to the limited time available, the requirements to meet test deadlines on all elements, and to support contract deliverables.

All devices were packaged in a special 28-pad leadless chip carrier (Fig. 5.2-1) with basic die bonding as shown in Fig. 5.2-2. Tables 5.2-2 and 5.2-3 list the packaged parts connections for the five major circuit devices, as listed in Table 5.2-1.

Table 5.2-1
Packaged Parts

Part No.	Function	JE1-14 No.	JE1-11 No.
D30457	4-bit up/down converter	31	51
D30458	÷ 6/7, 10/11, 20/21, 40/41 prescalers	9	7
D30459	4-bit accumulator	18	43
D30462	Phase detectors	24	36
D30463	4-bit shift register	17	19
Totals		99	166

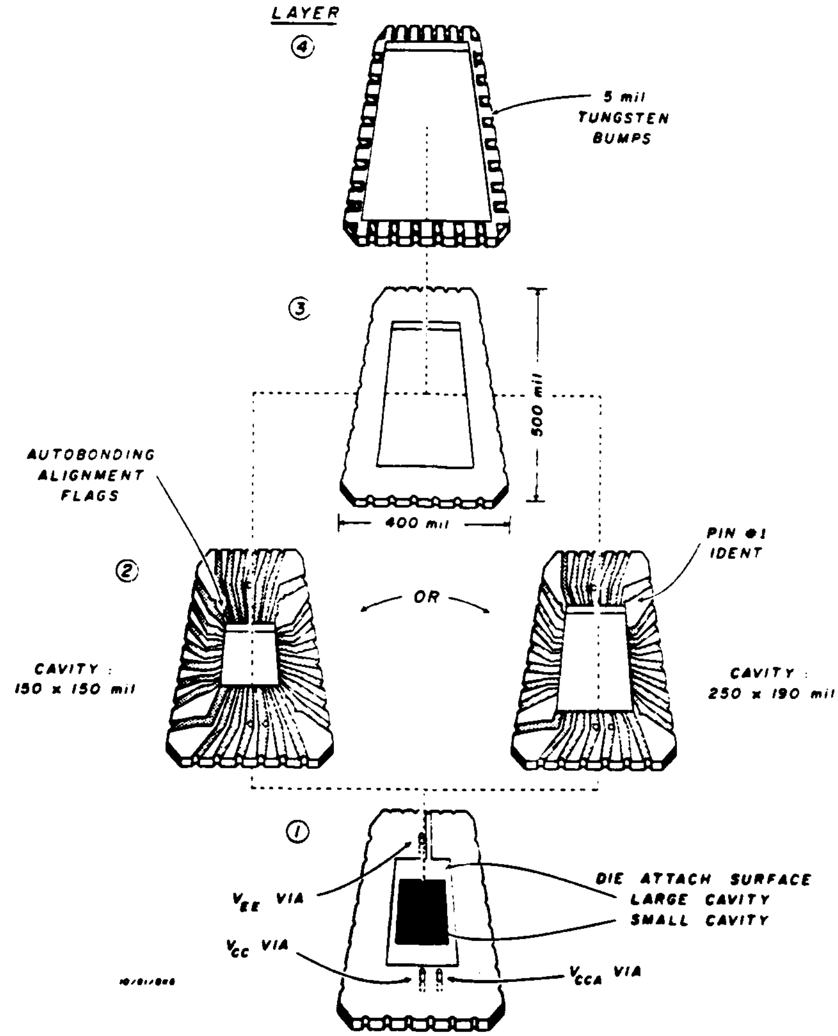


Fig. 5.2-1 GaAs technology insertion into DRFMs.

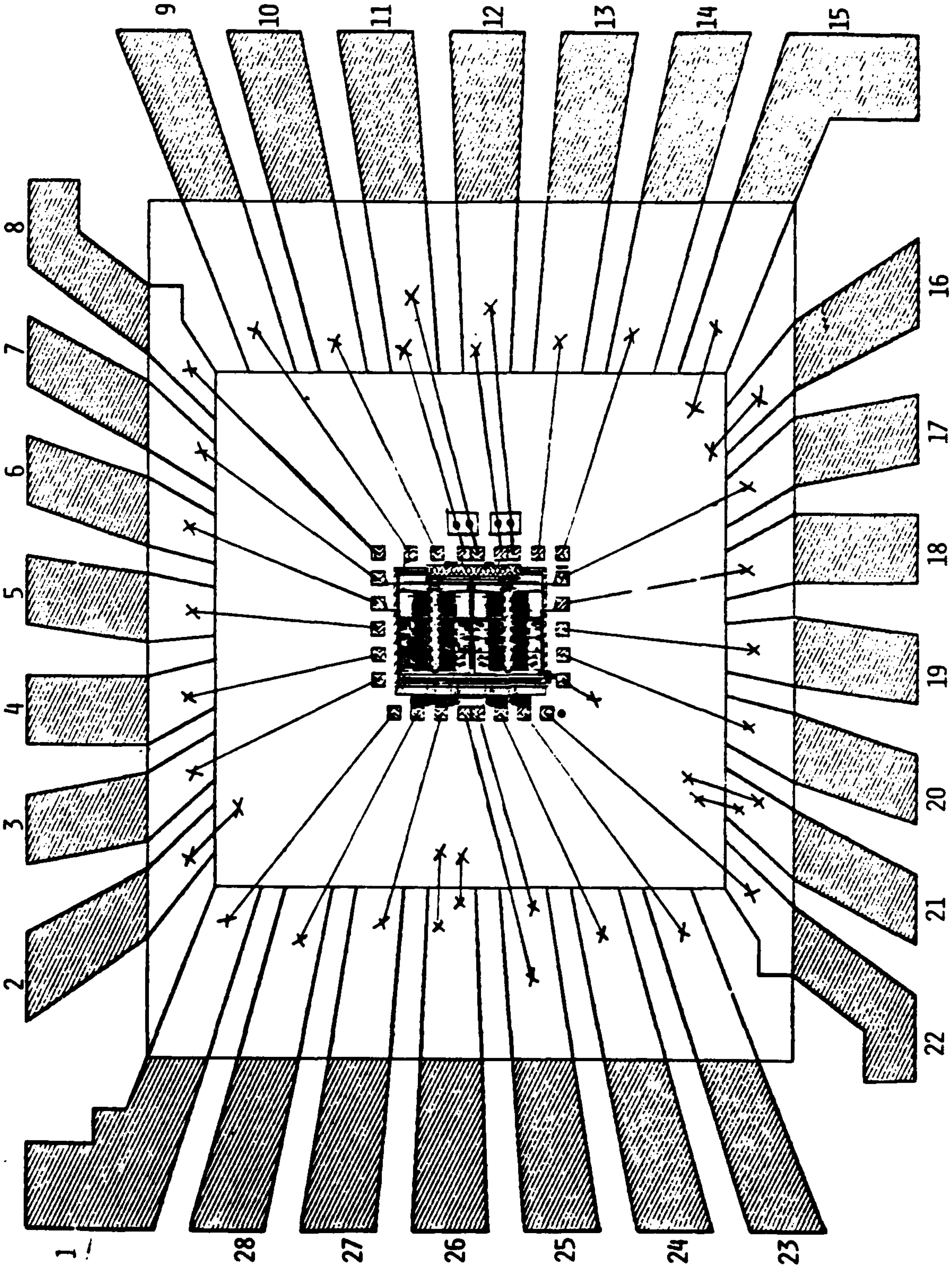


Fig. 5.2-2 MPFLA bonding diagram.

Table 5.2-2

Packaged Parts Connections

Connection Pad No.	Function: PN 30458 Mask Programmable Prescaler	Function: PN 30459 4-Bit Accumulator & ÷ 10/11
1	N.C.*	Carry out
2	Gnd	Gnd
3	N.C.	D3 in
4	N.C.	D2 in
5	N.C.	Carry in
6	÷ 40/41 control	D1 in
7	÷ 20/21 control	D0 in
8	N.C.	N.C.*
9	Clock	Accum reset
10	N.C.	Accum clock
11	V_{ss}	V_{ss}
12	V_{dd}	V_{dd}
13	N.C.	÷ 10/11 clock
14	N.C.	N.C.
15	Gnd	Gnd
16	Gnd	Gnd
17	÷ 10/11 control	÷ 10/11 control
18	÷ 6/7 control	N.C.
19	N.C.	N.C.
20	N.C.	N.C.
21	Gnd	Gnd
22	N.C.	÷ 10/11 output
23	÷ 6/7 output	Data out 3
24	÷ 10/11 output	Data out 2
25	V_{bb}	V_{bb}
26	Gnd**	Gnd**
27	÷ 20/21 output	Data out 1
28	÷ 40/41 output	Data out 1

* No connection

** If only one gnd connection, use this one

Table 5.2-3

Packaged Parts Connections

Connection Pad No.	PN 30457 4-Bit Up/Down Counter and ÷ 10/11	Function PN 30462 Type I & II Phase Detectors	PN 30463 4-Bit Shift Register and ÷ 10/11
1	Min/max count output	SFX out (2)	Data out 0
2	Gnd	Gnd	Gnd
3	D3 parallel input	N.C.	D3 parallel input
4	D2 parallel input	Variable freq. in (1)	DR serial input (right shift)
5	Serial input	N.C.	D2 parallel input
6	S2 control	N.C.	D1 parallel input
7	S1 control	Ref. freq. in (1)	DL serial input (left shift)
8	D1 parallel input	N.C.	D0 parallel input
9	D0 parallel input	N.C.	S2 control
10	U/D counter clock	N.C.	S1 control
11	V_{ss}	V_{ss}	V_{ss}
12	V_{dd}	V_{dd}	V_{dd}
13	÷ 10/11 clock	N.C.	÷ 10/11 clock
14	N.C.	N.C.	SR clock
15	Gnd	Gnd	Gnd
16	Gnd	Gnd	Gnd
17	÷ 10/11 control	Ref. freq. in (2)	÷ 10/11 control
18	N.C.	N.C.	N.C.
19	N.C.	N.C.	N.C.
20	N.C.	Variable freq. in (2)	N.C.
21	Gnd	Gnd	Gnd
22	÷ 10/11 output	N.C.	÷ 10/11 output
23	Data out 3	U1 out (1)	N.C.
24	Data out 2	D1 out (1)	Data out 3
25	V_{bb}	V_{bb}	V_{bb}
26	Gnd**	Gnd**	Gnd**
27	Data out 1	RFX out (2)	Data out 2
28	Data out 0	Lock output (2)	Data out 1

An accounting of yield after packaging and final test was not made due to the extensive testing involved. However, tests on the prescalers indicated five out of eight tested (60%) were fully functional, and nine out of 15 (60%) accumulator circuits were also fully functional at nominal operating voltages of:

V_{dd} = +2.8 V
V_{bb} = +2.8 V
V_{ss} = -2.0 V
Gnd = 0.0 V

5.3 Deliverables

Items delivered under this contract include:

5 prescalers (PN 30458)
8 4-bit accumulators (PN 30459)
1 high frequency test fixture
1 test instruction documentation

The ICs delivered to ERADCOM and associated data are listed in Table 5.3-1. All parts were selected from wafer JE1-14 which was proton-implanted to reduce backgating effects, as reported in Sec. 4.2.2.

Table 5.3-1

Parts Delivered to ERADCOM

Part No.	Name	Wafer	Power Supply Levels V_{DD}	V_{BB}	V_{SS}	Output Swing "0"	"1"	Frequency (MHz)	Functional (%)
4324	Prescaler 30458	JE1-14	2.8	2.8	-2	0.4 V	1.8	900	100
5324	Prescaler 30458	JE1-14	2.8	2.8	-2	0.5 V	2.0	900	100
5224	Prescaler 30458	JE1-14	2.8	2.8	-2	0.5 V	2.0	900	100
2224	Prescaler 30458	JE1-14	2.8	2.8	-2	0.5	2.0	800	100
2324	Prescaler 30458	JE1-14	2.8	2.8	-2	0.5	2.0	940	100
6223	Acc. 30459	JE1-14	2.8	2.8	-2	0.2	1.5	330	100
4223	Acc. 30459	JE1-14	2.8	2.8	-2	0.3	1.5	330	100
6353	Acc. 30459	JE1-14	2.8	2.8	-2	0.3	1.5	316	100
4353	Acc. 30459	JEi-14	2.8	2.8	-2	0.5	1.5	300	100
5323	Acc. 30459	JE1-14	2.8	2.8	-2	0.5	1.5	300	100
6253	Acc. 30459	JE1-14	2.8	2.8	-2	0.5	1.5	320	100
5323	Acc. 30459	JE1-14	2.8	2.8	-2	0.5	1.5	300	100
5344	Acc. 30459	JE1-14	2.8	2.8	-2	0.5	1.5	300	100

END